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A New SiC Planar-Gate IGBT for Injection Enhancement Effect and Low Oxide Field

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Abstract: A new silicon carbide (SiC) planar-gate insulated-gate bipolar transistor (IGBT) is proposed and comprehensively investigated in this paper. Compared to the traditional SiC planar-gate IGBT, the new IGBT boasts a much stronger injection enhancement effect, which leads to a low on-state voltage (V_{ON}) approaching the SiC trench-gate IGBT. The strong injection enhancement effect is obtained by a heavily doped carrier storage layer (CSL), which creates a hole barrier under the p-body to hinder minority carriers from being extracted away through the p-body. A p-shield is located at the bottom of the CSL and coupled to the p-body of the IGBT by an embedded p-MOSFET (metal-oxide-semiconductor field effect transistors). In off-state, the heavily doped CSL is shielded by the p-MOSFET clamped p-shield. Thus, a high breakdown voltage is maintained. At the same time, owing to the planar-gate structure, the proposed IGBT does not suffer the high oxide field that threatens the long-term reliability of the trench-gate IGBT. The turn-off characteristics of the new IGBT are also studied, and the turn-off energy loss (E_{OFF}) is similar to the conventional planar-gate IGBT. Therefore, the new IGBT achieves the benefits of both the conventional planar-gate IGBT and the trench-gate IGBT, i.e., a superior V_{ON}-E_{OFF} trade-off and a low oxide field.

Keywords: SiC planar-gate IGBT; injection enhancement effect; embedded trench p-MOSFET; carrier storage layer; E_{OFF}-V_{ON} trade-off

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1. Introduction

Silicon carbide (SiC) is attractive to power devices thanks to its superior material properties of wide bandgap, large critical electric field, high temperature endurance, etc. [1–6]. SiC-based power devices have been widely studied and commercially available: for example, metal-oxide-semiconductor field effect transistors (MOSFETs), and junction barrier Schottky diode. For quite high voltage power applications (>10 kV), SiC insulated-gate bipolar transistors (IGBTs) are preferred since bipolar conduction mode in the IGBTs can efficaciously reduce the on-state energy loss [7–13]. In traditional silicon technology, the trench-gate IGBT is widely used due to its injection enhancement effect which increases plasma density in the drift region [14–17]. However, in SiC technology, the SiC trench-gate structure suffers a high electric field of the gate oxide at off-state, because the critical electric field in SiC is about ten times higher than that of silicon [1]. The high gate oxide electric field in SiC trench power devices severely threatens the device reliability [18,19]. Too large of a gate oxide field extremely degrades the long-term reliability of the devices. It is found that under a high gate oxide electric field, hot carriers can be trapped in the gate oxide, leading to degraded device characteristics [20], and gate oxide breakdown easily happens with surface pit shape defects [21].

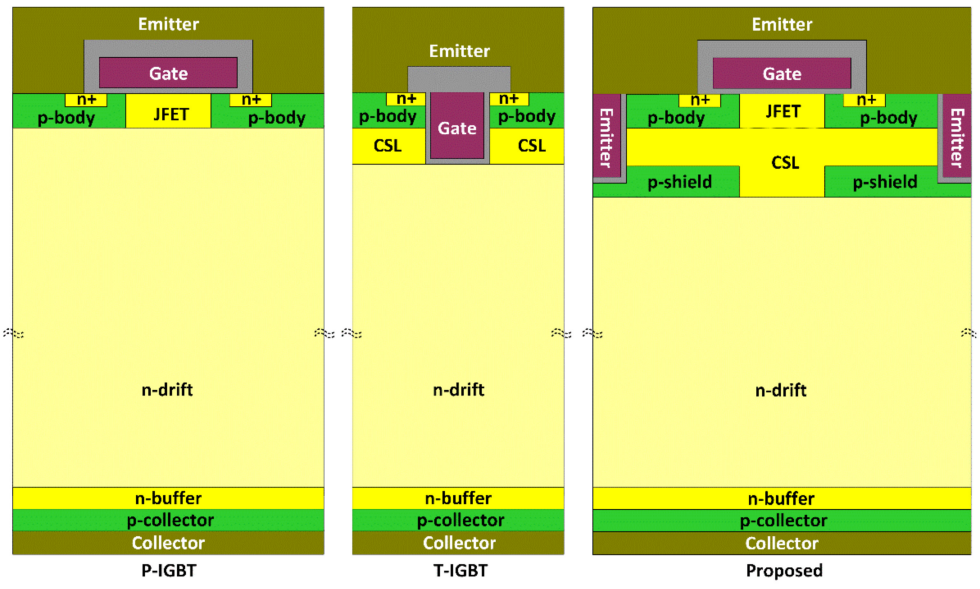
To decrease the high electric field in the gate oxide of the SiC trench-gate MOSFETs, grounded p-shields have been widely adopted [22,23]. However, for SiC trench-gate IGBT,

grounded p-shields will serve as hole extractors and dampen the conductivity modulation near the p-shield, which acts in opposition to the aim of trench-gate IGBTs. It was suggested that floating p-shields could maintain strong conductivity modulation in SiC trench-gate IGBTs [24,25]. However, a floating p-shield directly under the trench gate introduces concerns over electromagnetic interference (EMI) noise, which is widely reported in silicon IGBTs [26–28].

In this paper, a novel SiC planar-gate IGBT is proposed for injection enhancement effect. The IGBT features a heavily doped carrier storage layer (CSL), which enables a strong injection enhancement effect in the IGBT. A p-shield is located at the bottom of the CSL and is coupled to the p-body of the IGBT by an embedded trench p-MOSFET. Thus, the large off-state breakdown voltage is maintained. The proposed IGBT is systematically studied with Sentaurus TCAD simulations [3,29–31]. The essential physical models are included in this study: for example, doping dependent mobility, high-field saturation mobility, Auger and Shockley-Read-Hall (SRH) recombination, impact ionization, incomplete ionization of impurities, anisotropic mobility model, and band-gap narrowing. Based on the numerical simulations, the new IGBT structure is found to achieve the benefits of the conventional SiC planar-gate IGBT as well as SiC trench-gate IGBT, i.e., a superior V_{ON}-E_{OFF} trade-off and a low gate oxide field.

2. Device Structures and Static Characteristics

Figure 1 displays schematic cross-sections of the studied conventional SiC planar-gate IGBT (P-IGBT), SiC trench-gate IGBT (T-IGBT), and the new SiC planar-gate IGBT (proposed) in this study. In the proposed SiC IGBT, there is an embedded p-MOSFET which includes the p-body, CSL, p-shield under the p-body, the polysilicon in the trench, and the oxide in the trench. The studied IGBTs are designed to fulfil 20-kV voltage level power applications. The key parameters of the three IGBTs are same for comparison and are listed in Table 1. The doping density and thickness of the n-drift region are designed according to the 20-kV voltage level requirement. In the P-IGBT and the proposed SiC IGBT, the aperture of the JFET (junction field-effect transistor) region (i.e., distance between neighboring p-bodies) is 2 μm. The vertical distance between the p-body and the p-shield in the proposed IGBT is 3 μm.



(**a**) (**b**) (**c**)

Figure 1. Schematic cross-sections of (**a**) conventional SiC planar-gate insulated-gate bipolar transistor (IGBT) (P-IGBT), (**b**) SiC trench-gate IGBT (T-IGBT), and (**c**) the proposed SiC planar-gate IGBT (proposed).

Table 1. Parameters of the studied IGBTs.

Parameter	Value	Unit
Doping of n-drift	2.5×10^{14}	cm^{-3}
Thickness of n-drift	180	μm
Gate oxide thickness	50	nm
Channel mobility	30	$cm^2/V\text{-}s$
Channel length	1	μm
Doping of JFET	2×10^{16}	cm^{-3}
Doping of p-shield	1×10^{18}	cm^{-3}
Thickness of p-shield	1	μm
Doping of CSL	2×10^{16}	cm^{-3}

The static characteristics of the IGBTs are explored in this section. Firstly, the basic output characteristics of the three studied SiC IGBTs are investigated as well as compared. The on-state I_C-V_{CE} performance is shown in Figure 2. The gate-to-emitter voltage (V_{GE}) is set to be 15 V in on-state, which is the same as the gate drive voltage of Si MOSFET and IGBT for integration, conveniently. The on-state voltage V_{ON} of the studied SiC IGBTs is defined as the V_{CE} (when I_C is 50 A/cm^2 and V_{GE} is 15 V) in this paper. The V_{ON} of the P-IGBT is as high as 5.21 V, because the conductivity modulation in P-IGBT is weak due to the grounded p-bodies. This large V_{ON} will bring on-state energy loss in the application circuits and should be decreased. On the contrary to the P-IGBT, the T-IGBT obtains quite a lower V_{ON} of 3.44 V, which is only 66% of the V_{ON} of the P-IGBT. The low V_{ON} in the T-IGBT is owing to the enhanced injection enhancement effect, which enlarges the plasma density in the upper region of the T-IGBT. The higher plasma density in the upper region of the T-IGBT can be verified in Figure 3, which shows the plasma concentration along the vertical direction of the three investigated IGBTs. The T-IGBT has a plasma density of about 4×10^{15} cm^{-3} at the top side of the device, while the plasma density in the P-IGBT at the top side is smaller than the T-IGBT and even lower than 1×10^{15} cm^{-3}. As to the proposed SiC IGBT, the V_{ON} is 3.72 V, which is close to that of the T-IGBT and is much smaller than that of the P-IGBT. As shown in Figure 3, the plasma concentration in the upper region of this proposed IGBT is also quite higher than the plasma concentration of the P-IGBT, and close to the plasma density of the T-IGBT. The high plasma density in the proposed IGBT is owing to the heavily doped n-type CSL, which creates a hole barrier preventing the holes in the n-drift region to be extracted out. Hence, the high plasma density in the proposed IGBT enhances conductivity modulation and results in the lower V_{ON} of 3.72 V, which is only about 71% of the 5.21 V in the P-IGBT.

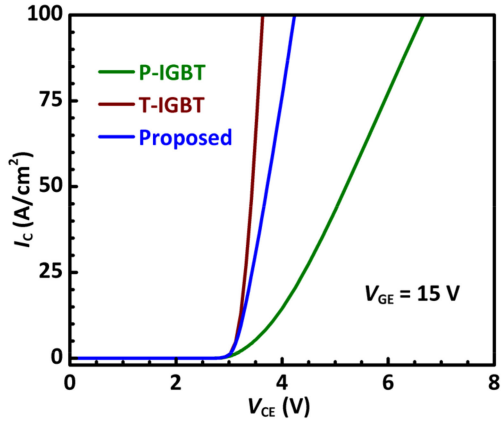


Figure 2. Output characteristics of the P-IGBT, T-IGBT, and the proposed SiC IGBT.

Although the heavily doped n-type CSL in the proposed SiC IGBT is the key to reduce V_{ON}, the CSL is also prone to weakening the blocking capability of the proposed IGBT. It is well known that the MOSFETs or IGBTs, featuring more heavily doped n-drift regions,

tend to have a lower breakdown voltage (BV). The electric field slope in a more heavily doped n-drift region is larger, and hence, the electric field at the junction between p-body and n-drift rises to critical breakdown electric field under only a small off-state collector voltage. Thus, the heavily doped n-type CSL beneath the p-body can be detrimental for the blocking capability of the proposed IGBT. To avoid blocking capability degradation, a new pn junction should be designed in the proposed IGBT. In this work, the p-MOSFET clamped p-shield under the CSL is designed as the key to maintaining the blocking capability of the proposed IGBT.

Figure 4 plots the BV performance of the three studied P-IGBT, T-IGBT, and the proposed IGBT, as well as the variation of the p-shield voltage ($V_{\text{p-shield}}$) in the proposed IGBT with the increasing of V_{CE} in off-state. All the three IGBTs have a very close BV of about 26 kV (BV is defined as the V_{CE} when collector current I_C is 1 A/cm^2 and V_{GE} is 0 V). The simulation results show, although the deep CSL exists in the proposed SiC IGBT, the blocking capability of the proposed SiC IGBT is not weakened. The reason comes from the turning-on of the embedded p-MOSFET, and the p-shield is coupled to the grounded p-bodies through the induced p-channel of the embedded p-MOSFET. In the proposed SiC IGBT, when the IGBT is switched off, the voltage of the p-shield increases with the collector voltage in the beginning of the switching process. When the voltage of the p-shield gets to the threshold voltage (V_{TH}) of the embedded p-MOSFET, the p-MOSFET is switched on with a p-channel induced between the p-body and the p-shield below. Then, the voltage of the p-shield is clamped at several volts (i.e., the voltage of the p-shield is almost the same as the threshold voltage $|V_{TH}|$ of the embedded p-MOSFET). With larger and larger off-state collector voltage V_{CE}, this off-state collector voltage will be sustained by the junction between the p-shield and lightly doped n-drift region, instead of the junction of the p-body and the heavily doped CSL. The voltage of the p-shield stays unchanged, as the p-shield is connected to the grounded p-body above. Before the breakdown of the IGBT, the voltage of the p-shield stays at only several volts. When V_{CE} is large enough and avalanche breakdown happens at the junction between p-shield and n-drift layers, the off-state avalanche current will increase soon in orders leading to a larger voltage of the p-shield. The inset in Figure 4 shows equipotential lines in the proposed IGBT at V_{CE} = 20 kV in off-state. The potential drop between two adjacent equipotential lines is 100 V, and the first equipotential line of 100 V is below the p-shield. Hence, it is clear that the main portion of the off-state voltage V_{CE} is blocked by the pn junction between the p-shield and n-drift in the proposed SiC IGBT. The potential of the CSL region is very low, as the p-shield is coupled to the grounded p-body and screens the CSL region from high electric field. Thus, the heavily doped CSL is protected by the p-MOSFET clamped p-shield. The BV of the proposed IGBT is about 26 kV and is not degraded, which is close to the BV of the other two IGBTs.

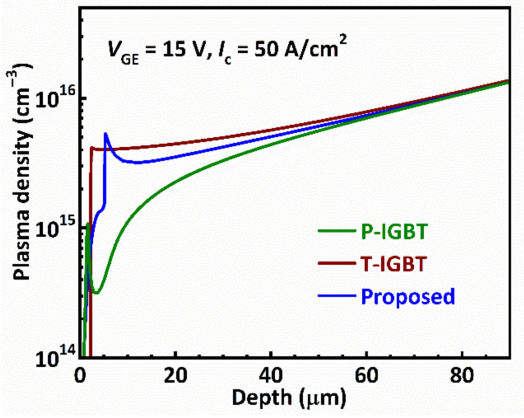


Figure 3. Plasma density in vertical direction of the studied P-IGBT, T-IGBT, and the proposed SiC IGBT at I_C = 50 A/cm^2.

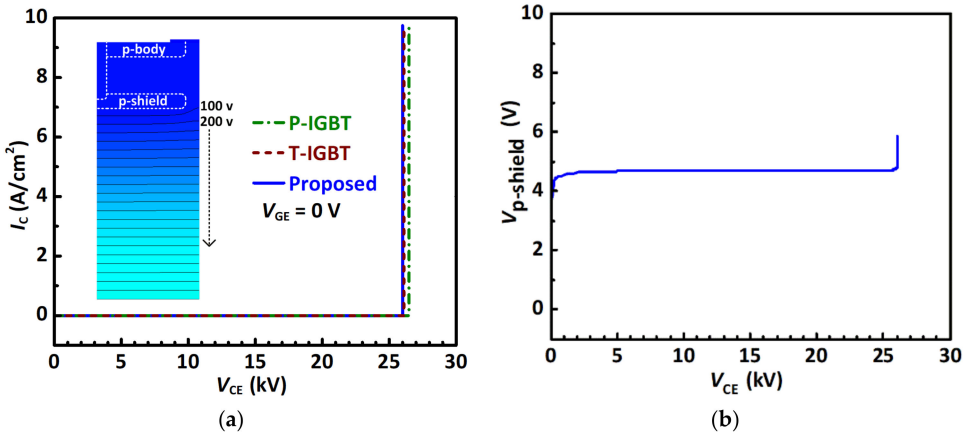


Figure 4. (**a**) *BV* performance. The equipotential lines (step = 100 V) of the proposed IGBT under V_{CE} = 20 kV are shown in the inset. (**b**) The variation of the p-shield voltage ($V_{p\text{-shield}}$) with the increasing of V_{CE} in the proposed SiC IGBT at off-state.

The strength of the gate oxide electric field is critical in SiC power devices. Too high of an electric field in the gate oxide of SiC power devices can reduce the lifetime of the devices. A high electric field in the gate oxide together with SiC surface defects easily lead to the breakdown of the gate oxide [21]. Under too high of a gate oxide electric field, hot carriers are prone to be trapped in the gate oxide, leading to the failure of power devices: for example, the threshold voltage shifting [20]. Since the critical breakdown electric field of SiC-based pn junction is about ten times of that of silicon, the SiC power devices in off-state can sustain a much higher electric field before breakdown. Consequently, the electric field in the gate oxide of the power devices tends to increase by the same proportion if identical device structures based on silicon are used. The electric field strength in the gate oxide often becomes the bottleneck for SiC power devices nowadays. Thus, a gate oxide electric field smaller than 3 MV/cm is widely required to guarantee the device reliability [32–34]. Figure 5 displays the off-state electric field distribution inside the studied P-IGBT, T-IGBT, and the proposed SiC IGBT under V_{CE} = 20 kV and V_{GE} = −5 V. In the P-IGBT, the p-bodies protect the gate bottom from the high off-state collector voltage. Electric field lines emitted from the depleted n-drift region mostly are terminated in the grounded p-bodies instead of the gate oxide. Hence, the maximum gate oxide electric field ($E_{ox\text{-}m}$) in the P-IGBT is small with only 2.14 MV/cm. While in the T-IGBT, whose gate protrudes beyond the grounded p-bodies, the gate oxide cannot be protected from the high off-state collector voltage. In this case, the electric field lines emitted from the depleted n-drift region mostly are terminated in the gate oxide instead of the grounded p-bodies, which is opposite to the P-IGBT. Thus, the gate oxide of the T-IGBT suffers a quite high maximum gate oxide electric field $E_{ox\text{-}m}$ of 8.89 MV/cm. Such a high $E_{ox\text{-}m}$ of 8.89 MV/cm is far beyond the acceptable level, and the T-IGBT could be broken within a short lifetime. In the proposed SiC IGBT, there are grounded p-bodies and also p-shields under the gate oxide. The off-state collector voltage V_{CE} of 20 kV is mainly supported by the junction between the p-shield and the lightly doped n-drift, as illustrated in the previous part explaining the blocking capability of the IGBTs. The electric field around the junction between p-shield and n-drift is highest in the proposed IGBT, and the region above the p-shield is well protected by the p-shield. The $E_{ox\text{-}m}$ of the proposed IGBT is only 1.05 MV/cm, which is far below the critical electric field of 3 MV/cm. In the proposed IGBT, the embedded p-MOSFET introduces a new trench MOS (metal-oxide-semiconductor) structure, and thus the gate oxide of the embedded p-MOSFET should also be investigated. As shown in the Figure 5, the $E_{ox\text{-}m}$ of the embedded trench p-MOSFET is very small with only 0.94 MV/cm and hence is not an issue for device reliability.

The operation mechanism of the proposed SiC IGBT in on-state as well as in off-state is summarized in Figure 6a,b. In on-state, the higher electron density in the heavily doped n-type CSL creates a high hole barrier. The CSL layer is connected to the grounded n+

emitter in on-state through the n-channel of proposed IGBT. So, the voltage of the CSL layer is also very small and almost zero. The embedded p-MOSFET is turned off in this situation, and no p-channel exists in the embedded p-MOSFET, as shown in Figure 6a. However, at off-state, the p-channel is formed in the proposed IGBT, as shown in Figure 6b. With the potential of p-shield and CSL layers increasing with the off-state collector voltage, the embedded p-MOSFET is turned on. Since the p-shield is connected to the grounded p-body through the induced p-channel, electric field lines emitted from the high voltage side are terminated in this p-shield to avoid the influence of the heavily doped CSL on blocking capability of the IGBT.

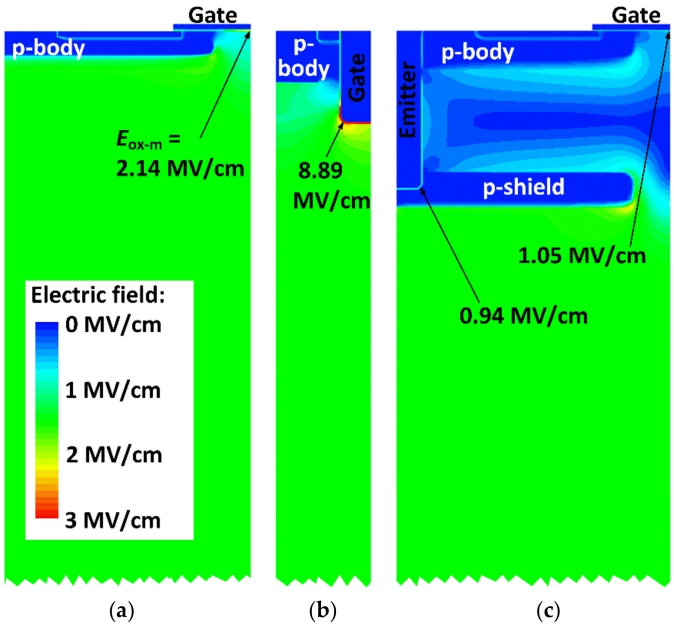


Figure 5. Off-state electric field distribution in the studied SiC IGBTs under V_{CE} = 20 kV and V_{GE} = −5 V. (**a**) P-IGBT. (**b**) T-IGBT. (**c**) The proposed SiC IGBT.

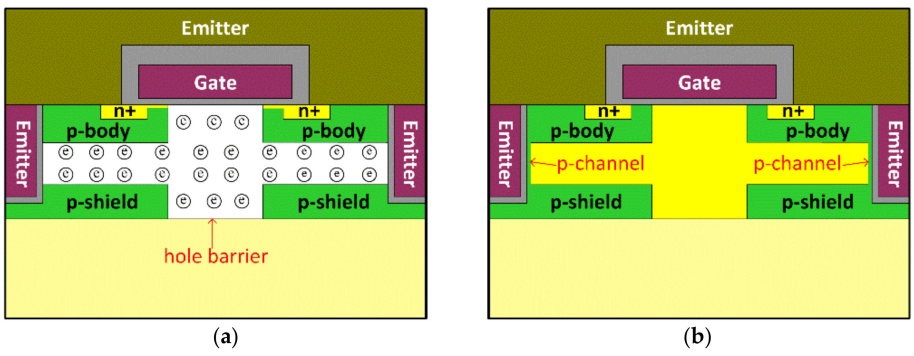


Figure 6. Operation mechanism analysis of the proposed IGBT in (**a**) on-state and (**b**) off-state.

The reverse transfer capacitance (C_{rss}) of a power transistor is also a significant device parameter for device reliability and is necessary to be analyzed [14]. When a power transistor is being switched off, the current decreases from the high on-state current to a very small off-state leakage current, while the collector or drain voltage of the transistor increases from a small on-state voltage to the high DC bus voltage. Although the gate voltage in this switching-off process decreases to be smaller than the threshold voltage of the transistor, the gate voltage is still affected by the increasing collector or drain voltage. Through the reverse transfer capacitance C_{rss}, the gate is coupled to the collector. The gate voltage is also increasing when the collector voltage is larger and larger in this switching-off process. This may result in false turning-on of the transistor, if the gate

voltage increases to be larger than the threshold voltage of the transistor again. A low C_{rss} is often desirable, since it can effectively suppress the false turn-on of the power transistors during switching operations, which otherwise would cause reliability issues of the power switching circuits [35]. Figure 7 presents the C_{rss} curves of the studied P-IGBT, T-IGBT, and the proposed SiC IGBT for comparison. The T-IGBT has a very large C_{rss}, because its trench gate protrudes beyond the p-body and hence is strongly coupled to the collector. Thanks to the screening effect from the grounded p-bodies to the planar gate, the P-IGBT has much smaller C_{rss} than the T-IGBT. The proposed IGBT has the lowest C_{rss} among the three studied IGBTs, since the p-body and p-shield collectively screen the planar gate from being affected by the collector.

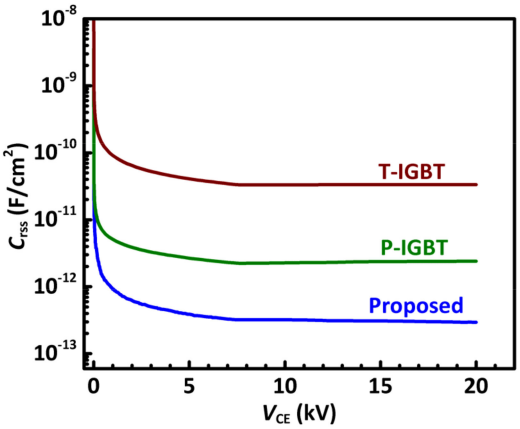


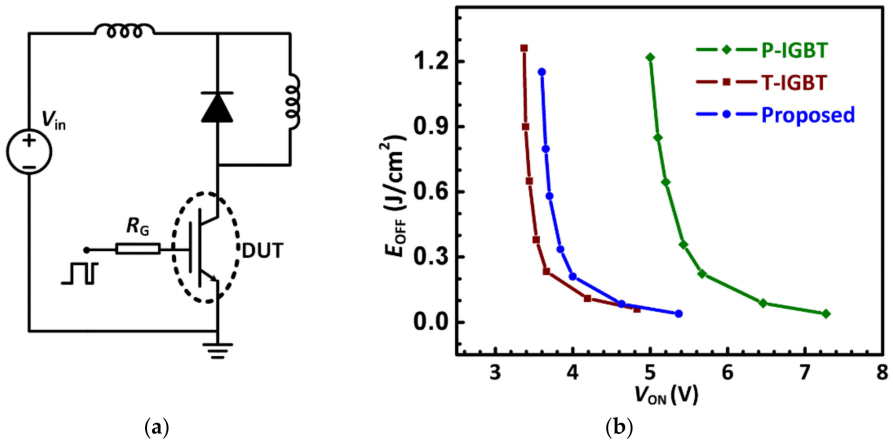
Figure 7. Reverse transfer capacitance (C_{rss}) of the studied P-IGBT, T-IGBT, and the proposed SiC IGBT.

3. Dynamic Characteristics

As shown in the above section, the proposed SiC IGBT has obtained a low on-state voltage V_{ON} approaching that of the T-IGBT, because the heavily doped carrier storage layer creates a hole barrier in the upper region of the proposed SiC IGBT. The V_{ON} of an IGBT is a trade-off parameter with the switching-off energy loss (E_{OFF}), since stronger conductivity modulation that reduces V_{ON} also demands a longer switching time to remove the large number of minority carriers. To study switching-off transient performances of the investigated SiC IGBTs, the schematic circuit in Figure 8a is used for the simulations. The DC bus voltage V_{in} is 13 kV in the circuit. The IGBT is the device under test (DUT). Areas of the active devices (the DUT and the diode) are set to be 1 cm^2. The parasitic inductance in the power loop is assumed to be 10 nH. The gate resistance R_G is set as 10 Ω. The V_{GE} is set to be between −5 V and +15 V. To study the switching-off process of the IGBTs, the V_{GE} decreases from +15 V to −5 V to turn off the IGBTs.

As illustrated above, excessive minority carriers shown in Figure 3 help to enhance the conductivity modulation in the T-IGBT and the proposed IGBT. These carriers need to be moved out from the n-drift region in switching-off transient, because the n-drift region needs to be in a depleted state to bear off-state collector voltage. The turn-off energy loss E_{OFF} is calculated by the product of current I_C and voltage V_{CE}. Hence, the E_{OFF} of the IGBTs mainly occurs in the high-power duration, i.e., the time duration when a high voltage drop of the IGBT and a high current flowing through the IGBT coexist. The E_{OFF} is not useful in realizing the function of the application circuit and adds up to more energy waste. The T-IGBT and the proposed IGBT have larger plasma density in their upper region, which may increase the E_{OFF}. However, the simulation results in Figure 8 disclose this part of plasmas in the T-IGBT and the proposed IGBT does not obviously increase its switching-off energy loss. During the switching-off transient, the plasmas in the upper region of the IGBTs are extracted out before the extraction of the plasmas in the middle and bottom sides of the IGBTs. Before the plasmas in the top side of the IGBTs have been moved out of the devices and the top side region has been depleted, the collector voltage has not

been built up in pn junctions, i.e., V_{CE} is very low at this stage. The product of the low V_{CE} and the current flowing through the device is also quite small. Therefore, this period in the switching-off transient has very limited influence on the total E_{OFF}. Hence, the T-IGBT and the proposed SiC IGBT show similar E_{OFF} with the P-IGBT, although the distributions of plasmas among them are different at the upper regions. Figure 8b shows the trade-off performance between the E_{OFF} and V_{ON} in the studied IGBTs. The doping density of the p-collector is varied to adjust the injection efficiency in each IGBT. A higher p-collector dose (i.e., the product of p-collector doping density and p-collector thickness) is beneficial to obtain larger injection efficiency, but the excessive minority carriers injected from p-collector into n-drift also increase the E_{OFF}. The results in Figure 8b show that the T-IGBT and proposed IGBT boast better E_{OFF}-V_{ON} trade-off relationship than P-IGBT. Therefore, the proposed IGBT exhibits both superior static and dynamic characteristics.



(**a**) (**b**)

Figure 8. (**a**) Schematic of the circuit for simulating switching characteristics. (**b**) E_{OFF}-V_{ON} trade-off characteristics of the studied P-IGBT, T-IGBT, and proposed IGBT with changing the doping density of the p-collector region.

In power applications, the transistors work as switches and need to be turned on and off periodically. The characteristics of the proposed SiC IGBT experiencing multi-cycle switching process are necessary to be investigated. For unipolar power devices, e.g., SiC power MOSFET, it has been found that floating p-regions bring degradation in the conduction property of the device, due to the negative charges stored in floating p-regions [36–38]. In off-state, the floating p-regions are depleted, and the remaining negative charges in the floating p-regions help to bear the off-state drain voltage. However, in the following on-state period, the negative charges stored in the floating p-regions cannot be discharged with only electron current in MOSFETs. For the bipolar IGBTs, the floating p-regions are widely adopted for various purposes [39,40].

In this paper, the p-shield of the proposed IGBT is not grounded, and the device performance under multi-cycle switching process should be studied. Figure 9 shows multi-cycle switching curves (I_C and V_{CE}) of the proposed SiC IGBT. In the set-up, the V_{GE} (not shown in Figure 9) is a square wave with +15 V in half time of a cycle to turn on the proposed IGBT, and −5 V in the other half time of the cycle to turn off the proposed IGBT. As displayed in Figure 9, when the current I_C increases in every on-state period in a cycle, the corresponding V_{CE} of the IGBT increases and equals the V_{ON} at the same I_C in Figure 2. When the I_C is 50 A/cm^2, the V_{CE} of the proposed IGBT is 3.72 V and is the same as the V_{ON} shown in the static characteristics in Figure 2. Thus, unlike the unipolar SiC power MOSFET with floating p-regions, the proposed SiC IGBT as a bipolar device does not suffer a dynamic degradation although the p-shield is not grounded. Same as the MOSFETs, negative charges exist in the p-shields of the proposed SiC IGBT in off-state. However, in the next on-state process, the holes injected from the p-collector of the IGBT

can efficiently discharge the stored negative charges in the previous off-state process in multi-cycle switching.

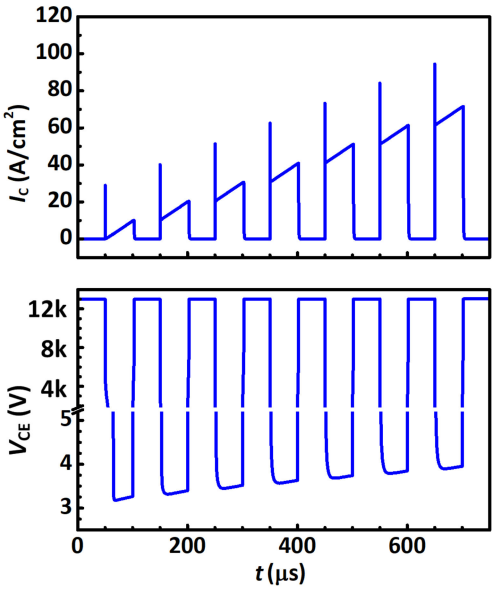


Figure 9. Multi-cycle switching curves (I_C and V_{CE}) of the proposed IGBT.

4. Proposed Fabrication Procedure

A feasible fabrication procedure of the new SiC IGBT is proposed with a set of established process steps in conventional planar gate SiC IGBT [12,41–43]. The proposed fabrication flow is illustrated in Figure 10. The fabrication starts with a SiC substrate with epitaxial n-drift layer. On the n-drift layer, the more heavily doped n-layer can be formed by epitaxial growth or ion implantation. Then p-shield regions are formed by ion implantations. All the implantation should be followed by high-temperature annealing in argon gas. Then, an n-type SiC layer is regrown [42,43], following which, the p-body regions and n+ regions are formed by ion implantations. Then, the trenches are created by dry etching, followed by gate oxide growth or deposition. Post-oxidation annealing is required to obtain a high-quality oxide/SiC interface. A polysilicon layer is then deposited. The planar-gate region is masked, and the polysilicon is etched back; the planar gate of the proposed IGBT and the trench gate of the embedded p-MOSFET are formed simultaneously in this step. The polysilicon and gate oxide can be etched with ICP (inductively coupled plasma etching) or RIE (reactive-ion etching), followed by high-temperature annealing. Then, dielectric isolation and metallization for contacts are carried out.

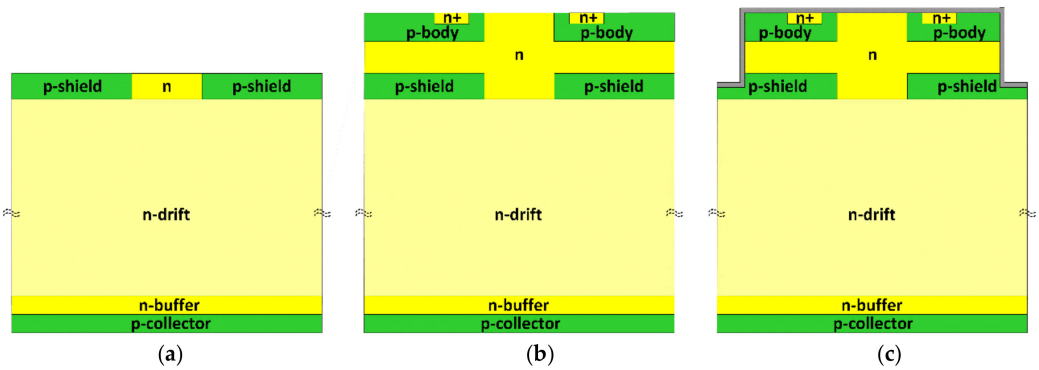


Figure 10. *Cont.*

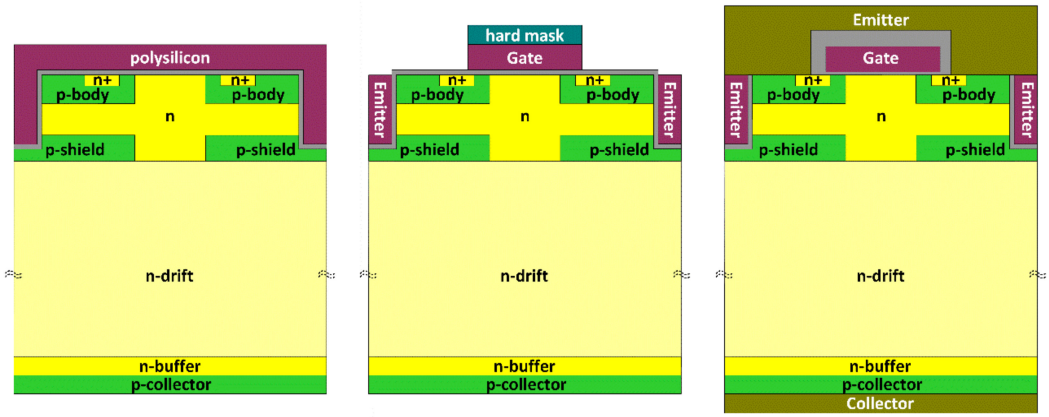


Figure 10. Proposed fabrication procedure for the new SiC IGBT: (**a**) p-shield formation by implantation; (**b**) n-layer regrown, n+-source, and p-body implantation; (**c**) gate oxide formation; (**d**) polysilicon deposition; (**e**) etching-back of polysilicon; (**f**) isolation and contact.

5. Conclusions

We propose a novel silicon carbide (SiC) planar-gate insulated-gate bipolar transistor (IGBT) with embedded p-MOSFETs. In on-state, the proposed SiC IGBT boasts a very strong injection enhancement effect owing to a heavily doped carrier storage layer (CSL) that creates a hole barrier around the p-body. To maintain a breakdown voltage (*BV*) high enough for 20-kV level power applications, a p-shield is located at the bottom of the CSL and coupled to the p-body of the IGBT to terminate the high electric field from the collector side. The *BV* of the proposed IGBT is about 26 kV. Owing to the planar-gate structure and the p-MOSFET clamped p-shield, the proposed SiC IGBT has a very low gate oxide electric field of 1.05 MV/cm in off-state. Thus, the new IGBT combines benefits of the conventional planar-gate IGBT (P-IGBT) as well as the conventional trench-gate IGBT (T-IGBT): it simultaneously achieves a superior V_{ON}-E_{OFF} trade-off and a low gate oxide field. Therefore, the proposed SiC IGBT is a promising candidate as a switch for ultrahigh voltage power switching applications.

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