energies

MDPI

Article

Stacked Buck Converter: Current Ripple Elimination Effect and Transient Response

Chien-Chun Huang [1], Yu-Chen Liu [2], Chia-Ching Lin [1], Chih-Yu Ni [1] and Huang-Jen Chiu [1,*]

[1] Department of Electronic and Computer Engineering, National Taiwan University of Science and Technology, Taipei 10607, Taiwan; u8910659@gmail.com (C.-C.H.); harry131131@gmail.com (C.-C.L.); et85961028@gmail.com (C.-Y.N.)
[2] Department of Electronical Engineering, National Ilan University, Ilan 260007, Taiwan; ycliu@niu.edu.tw
* Correspondence: hjchiu@mail.ntust.edu.tw; Tel.: +886-27376419

Abstract: To balance the cost and volume when applying a low output current ripple, the power supply design should be able to eliminate the current ripple under any duty cycle in medium and high switching frequencies, and considerably reduce filter volume to improve power density. A stacked buck converter was eventually selected after reviewing the existing solutions and discussing their advantages and disadvantages. A stacked buck converter is used as a basis to propose the transient response and output current ripple elimination effect, boundary limit control method, and low output ripple dead time modulation method to make individual improvements. The principle, mathematical derivation, small-signal model, and compensator design method of the improvement method are presented in detail. Moreover, simulation results are used to mutually verify the correctness and effectiveness of the improvement method. A stacked buck converter with 330-V input, 50-V output, and 1-kW output power was implemented to verify the effect of the low output current ripple dead time modulation. Experimental results showed that the peak-to-peak value of the output current ripple was reduced from 2.09 A to 559 mA, and the RMS value was reduced from 551 mA to 91 mA, thereby effectively improving the output current ripple.

Keywords: stacked buck; current ripple cancellation; transient response

Citation: Huang, C.-C.; Liu, Y.-C.; Lin, C.-C.; Ni, C.-Y.; Chiu, H.-J. Stacked Buck Converter: Current Ripple Elimination Effect and Transient Response. *Energies* **2021**, *14*, 64. https://dx.doi.org/10.3390/en14010064

Received: 22 November 2020
Accepted: 21 December 2020
Published: 24 December 2020

1. Introduction

With the development of technology, batteries have been extensively used in daily life. Batteries are used in electric vehicles [1–3], wearable devices, and large energy storage systems [4–6]. Therefore, the efficiency, life, and reliability of batteries are becoming increasingly critical. A battery management system (BMS) [7–9] is widely used to improve the utilization of batteries. Apart from preventing overcharge and over-discharge of batteries, BMS diagnoses and analyzes battery life and health status by recording battery-related data and residual capacity to optimize their overall performance.

One of the standard test methods for batteries' usable capacity is the coulomb measurement method [10,11]. This method is used to calculate the current value flowing into or out of batteries and integrates the current value over time to determine the number of coulombs flowing through. This method can accurately estimate the available battery capacity. In battery capacity measurement, the accuracy of voltage and current measurements is related to the final calculation error. To achieve an accurate battery capacity calculation, the battery charging current must be accurately measured. The current ripple elimination mechanism is particularly important to prevent the output current ripple from causing measurement errors and reduce the volume of the output capacitor to increase power density.

Standard current ripple elimination techniques are mainly divided into three categories. The first category uses multi-phase buck converters in parallel and alternately switched with one another [12,13]. Through the sum of the current ripples of different phases, the final synthesized overall output current can reduce the total ripple amount and

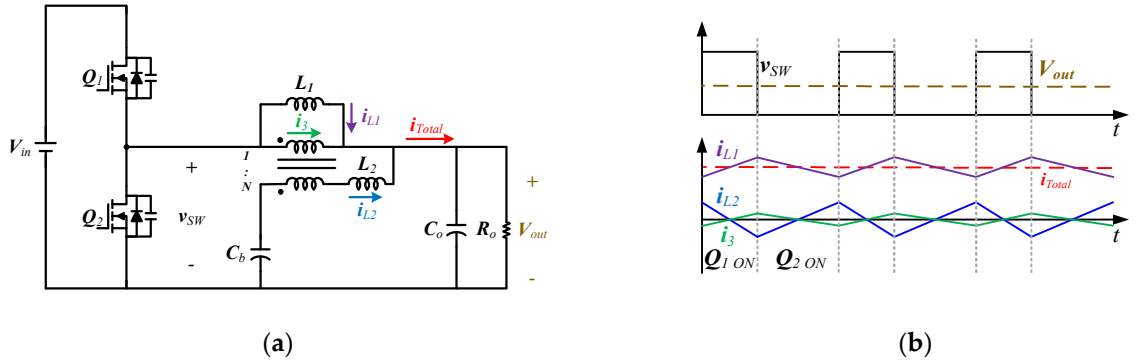
period, thereby increasing the equivalent current ripple frequency to reduce the capacitance of the output capacitor. However, the combined current ripples with this approach can only cancel each other under a specific duty cycle and number of parallel connections, thereby achieving an ideal current ripple elimination effect. Moreover, the use of multiple units in parallel increases the circuit cost and layout area, and the current sharing between multiple converters also requires additional control [14,15], thereby increasing the overall complexity. The second category uses coupled inductors to generate reverse ripple current [16,17]. The coupled inductor automatically generates the reverse ripple current, and the current ripple cancellation function can be achieved under any duty cycle. However, this cancellation function is fundamentally a fourth-order LC filter [18], which is based on filtering to obtain the characteristics of low output current ripple. A converter's output current filtering capability and transient response often have opposite design indicators when designing a fourth-order LC filter. To achieve a superior filtering effect, the inductance value of the filter should be increased, which directly reduces the transient response speed of the converter. Therefore, the converter's transient response will be fundamentally limited in the application of low current ripple output. The third category uses a stacked architecture [19,20], which utilizes the complementary operation of the upper and lower switches of the two bridge arms to superimpose the two arms' inductor currents. In this way, the output inductor current ripple can be canceled under any switching duty cycle. This architecture can accelerate the rising or falling slope of the overall output current when both arms are turned on simultaneously on the upper or lower bridge switch, thereby improving the transient response. However, the literature [19,20] has only extensively discussed complementary switching signals. Moreover, these studies have not focused on the dead time of the upper and lower bridge switching signals in practical applications and the parasitic capacitance of switching elements. Consequently, the current ripple elimination effect is affected. The RC delay control method proposed in the pattern [21] improves the transient response by increasing a converter's transient response. However, this method has flaws. After the feedback compensator is saturated, the area where the switching signals of the two arms overlap simultaneously cannot be generated, and the ability to increase the transient response is lost. On the basis of the preceding literature discussion, this study proposes a low output ripple dead time modulation and boundary limit control methods to improve the stacked buck converter's output current ripple elimination effect and increase the transient response.

The remainder of this paper is structured as follows. Section 1 presents the research background and introduction. Section 2 reviews the two architectures proposed in the literature [16,17] and briefly describes their operating principles. Thereafter, the coupling mutual inductance form is converted into a fourth-order LC filter form [18]. The fourth-order filter is used to illustrate why the output current ripple filtering ability and transient response cannot be considered. Section 3 reviews the stacked buck converter [19] and explains its operation and current ripple elimination principle. Moreover, this section uses the perspective of large signals to describe the fastest response speed that the converter can provide when the signals overlap simultaneously. Section 4 reviews the RC delay control method [21] and explains its limitations. Thereafter, this restriction is used as a basis to propose a new type of control method called the boundary limit control method. Section 4 also explains its principle and uses simulation to verify the effect of the boundary limit control method. Section 5 presents the influence of the switching dead time and switching parasitic capacitance of the stacked buck converter on the current ripple elimination effect and proposes a mathematical analysis of the principle. The dead time modulation method and formulation of the modulation variables are verified using mathematical derivation and simulation to confirm the feasibility and effectiveness of this modulation method. Section 6 organizes the small-signal model of the coupled-inductor stacked buck converter. The small-signal model contains the small-signal model under the general two-arm switch complementary operation and boundary limit control method to design closed-loop compensation. Lastly, simulations are used to show the transient response

of the system under different compensators. Section 7 implements a sample circuit. This section likewise measures the effect of the switching dead time modulation method on the current ripple elimination ability. Lastly, Section 8 summarizes this research.

2. Review of the Two Architectures and the Process of Converting Them to a Fourth-Order LC Filter

Figure 1 shows the circuit architecture and operation sequence diagram of the Ripple Current Cancellation Circuit (RCCC) [16]. The entire architecture includes a blocking capacitor C_b, coupled inductor, primary side magnetizing inductance L_1, secondary side equivalent leakage inductance L_2, and the primary and secondary turns ratio of 1:N.



(**a**) (**b**)

Figure 1. Ripple current cancellation circuit: (**a**) circuit architecture diagram; (**b**) operation sequence diagram.

From the steady-state volt-second balance of the equivalent leakage inductance L_2, the voltage on C_b can be deduced to equal the output voltage V_{out}. If C_b and C_{out} are assumed to be sufficiently large to disregard the voltage ripple on the capacitor, then the equations for i_{L1}, i_{L2}, and i_3 can be derived as follows:

$$\frac{di_{L1}}{dt} = \frac{v_{SW} - V_{out}}{L_1}, \tag{1}$$

$$\frac{di_{L2}}{dt} = -N\frac{L_1}{L_2}\frac{di_{L1}}{dt}, \tag{2}$$

$$\frac{di_3}{dt} = -N\frac{di_{L2}}{dt}. \tag{3}$$

To satisfy the ripple of the output current to zero amperes, the equation should be as follows:

$$\frac{di_{L1}}{dt} + \frac{di_{L2}}{dt} + \frac{di_3}{dt} = 0. \tag{4}$$

By substituting Equations (1)–(3) into Equation (4), the relational equation can be derived as follows:

$$N^2 - N + \frac{L_2}{L_1} = 0. \tag{5}$$

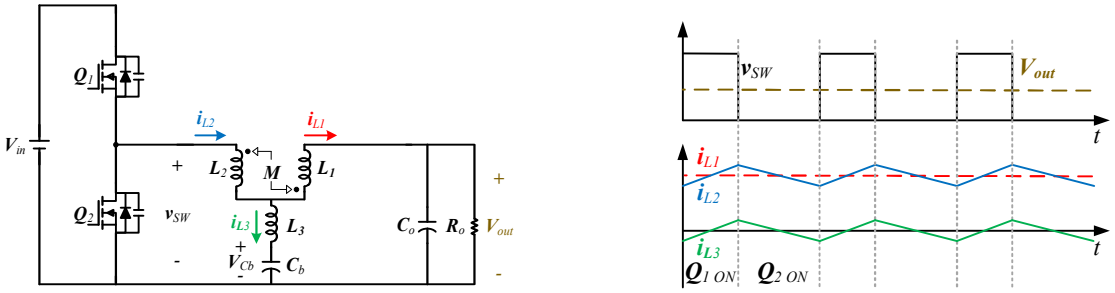
From Equation (5), N can be obtained as follows:

$$N = \frac{1}{2} \pm \sqrt{\frac{1}{4} - \frac{L_2}{L_1}}. \tag{6}$$

When N satisfies Equation (6) in the RCC architecture, the output current can obtain the best elimination effect.

Figure 2 shows the circuit architecture diagram and operation sequence diagram of the three-terminal LL-LC network for current ripple cancellation (LL-LC) [17]. The entire LL-LC architecture includes a blocking capacitor C_b, coupled inductor, primary

self-inductance L_1, secondary side self-inductance L_2, and a mutual inductance M between the primary side and secondary side winding, and an external inductor L_3.



(**a**) (**b**)

Figure 2. LL-LC circuit: (**a**) circuit architecture diagram; (**b**) operation sequence diagram.

Figure 2 also shows that through the operating interval when switches Q_1 and Q_2 are turned on, Equations (7) and (8) can be respectively written as follows:

$$(L_2 + M)\frac{di_{L2}}{dt} + (L_1 + M)\frac{di_{L1}}{dt} = V_{in} - V_{out}, \tag{7}$$

$$(L_2 + M)\frac{di_{L2}}{dt} + (L_1 + M)\frac{di_{L1}}{dt} = -V_{out}. \tag{8}$$

According to Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL), the following two equations can be obtained:

$$i_{L2} = i_{L1} + i_{L3}, \tag{9}$$

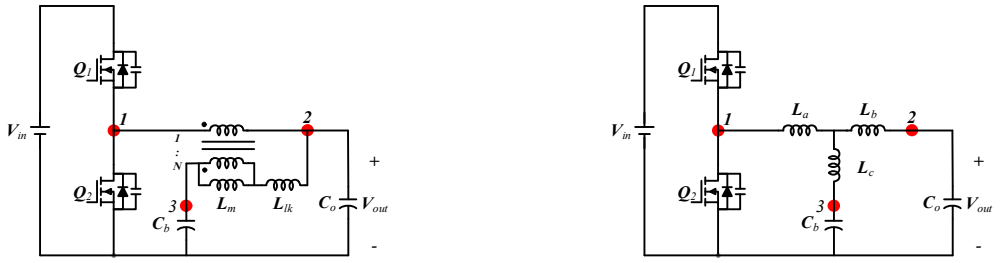
$$(L_1 + M)\frac{di_{L1}}{dt} - (L_3 - M)\frac{di_{L3}}{dt} = V_{Cb} - V_{out}. \tag{10}$$

In a steady-state operation, the average voltage across the inductor is zero. Hence, the voltage across V_{Cb} is equal to the output voltage V_{out}. Assuming that the C_3 capacitor is sufficiently large, its ripple can be disregarded. Equation (10) can be rewritten as follows:

$$(L_1 + M)\frac{di_{L1}}{dt} - (L_3 - M)\frac{di_{L3}}{dt} = 0. \tag{11}$$

When the inductance designed by L_3 is equal to the mutual inductance M, the current change of i_{L1} in Equation (11) must be zero to satisfy this equation. Hence, i_{L1} can achieve the function of eliminating the current ripple.

RCCC and LL-LC can achieve zero current ripple output under the condition that the voltage ripple on the blocking capacitor is disregarded, and the ideal winding turns ratio and external inductance are ideally matched. However, this conclusion must be established on the fact that voltage ripple on blocking capacitor C_b is minimal, and C_b is simplified as a constant voltage source. In addition, the capacitance value is finite, given the blocking capacitor in the actual circuit. Given that the voltage ripple on the blocking capacitor must be considered, the two architectures' actual effects on the elimination of the output current ripple should be re-discussed. A review of the circuit structure diagram of RCCC shows that the primary side inductance is equivalent to the secondary side, and the name of the capacitor and inductance is changed, as shown in Figure 3a. Furthermore, Figure 3b shows that the RCCC equivalent circuit diagram of the transformer model changed to the T equivalent model.



(**a**) (**b**)

Figure 3. Ripple current cancellation circuit: (**a**) transformer type; (**b**) T-type equivalent form.

To make a conversion between the transformer and T-type equivalent models, the three nodes marked on the transformer in Figure 3 must be described, and the impedance of any two nodes should be observed. Hence, the following three equations can be obtained:

$$L_a + L_b = \frac{L_m}{N^2}, \tag{12}$$

$$L_b + L_c = L_m + L_{lk}, \tag{13}$$

$$L_a + L_c = \left(1 - \frac{1}{N}\right)\left(\frac{N-1}{N}L_m\right) + L_{lk}. \tag{14}$$

Equations (12)–(14) show that L_a, L_b, and L_c can be derived as follows:

$$L_a = \frac{-L_m(N-1)}{N^2}, \tag{15}$$

$$L_b = \frac{L_m}{N}, \tag{16}$$

$$L_c = L_m - \frac{L_m}{N} + L_{lk}. \tag{17}$$

In rewriting Equation (5), set $L_1 = N^{-2}L_m$, $L_2 = L_{lk}$, then:

$$N^2 - N + \frac{N^2 L_{lk}}{L_m} = 0. \tag{18}$$

The following equation is obtained when Equation (18) is substituted into Equation (17):

$$\begin{aligned} L_c &= L_m - \tfrac{L_m}{N} + L_{lk} \\ &= \tfrac{L_m}{N^2}\left(N^2 - N + \tfrac{N^2 L_{lk}}{L_m}\right) \\ &= 0. \end{aligned} \tag{19}$$

From the result of Equation (19), L_c in the T-type model will become zero. The entire RCCC circuit will be converted into an LCLC fourth-order filter architecture, as shown in Figure 4.

Using the same method, the coupled inductor in LL-LC is converted to a T-type model, as shown in Figure 5.

To make a conversion between the transformer and T-type equivalent models, the three nodes marked on the transformer in Figure 5 are described, and the impedance of any two nodes is presented. Thus, the following three equations can be obtained:

$$L_a + L_b = L_1 + L_2 + 2M, \tag{20}$$

$$L_b + L_c = L_1, \tag{21}$$

$$L_a + L_c = L_2. \tag{22}$$

Equations (20)–(22) show that L_a, L_b, and L_c can be deduced as follows:

$$L_a = L_2 + M, \tag{23}$$

$$L_b = L_1 + M, \tag{24}$$

$$L_c = -M. \tag{25}$$

Comparing the design in Equations (11) and (25), when $L_3 = M$, then:

$$\begin{aligned} L_3 + L_c &= M - M \\ &= 0. \end{aligned} \tag{26}$$

The result of Equation (26) indicates that if the design conditions of LL-LC are met, then L_c and L_3 in the T model will cancel each other out to zero. Furthermore, the entire LL-LC circuit will be converted into an LCLC fourth-order filter architecture, as shown in Figure 6.

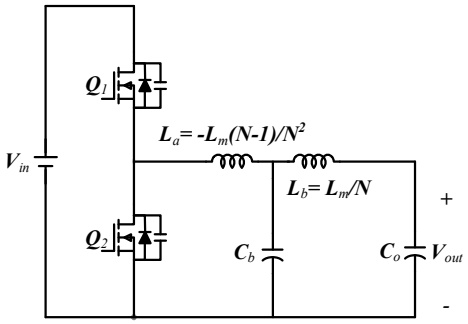


Figure 4. Structure diagram of the equivalent fourth-order LCLC filter of the RCCC circuit.

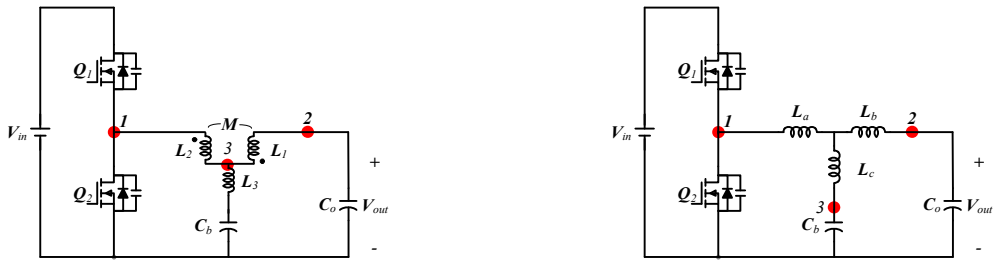


Figure 5. LL-LC circuit: (**a**) transformer type; (**b**) T-type equivalent form.

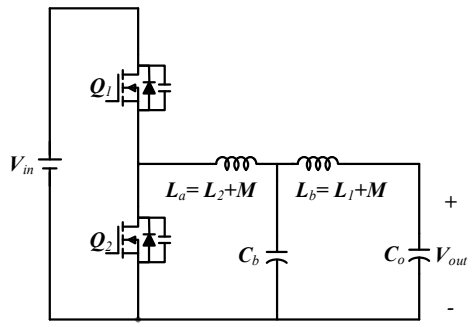


Figure 6. Structure diagram of the equivalent fourth-order LCLC filter of the LC-CC circuit.

Two things can be learned in comparing the results of the conversion of RCCC and LL-LC into an equivalent fourth-order LCLC filter in Figures 4 and 6. First, if the specific design conditions are met, then RCCC and LL-LC are essential fourth-order LCLC filters. Second, the ratios of L_a and L_b in the two equivalent fourth-order LCLC filters are not the same, but both have the function of current ripple filtering.

Given a fourth-order filter structure, the final filtering result of the output current ripple is determined by two aspects: (1) amount of ripple of the L_a inductor current and (2) ripple split ratio of L_b and C_b. To achieve an excellent current ripple filtering result, the inductance value of L_a should be considerably increased to reduce the inductance and capacitance values required by the current sharing circuit composed of L_b and C_b. Therefore, to pursue an excellent current ripple filtering effect for a fourth-order filter, the component value of the filter should be increased. However, such a design inevitably reduces the transient response of the converter.

3. Review of the Stacked Buck Converter

Figure 7 shows the circuit structure and operation sequence diagram of the stacked buck converter [19]. Q_1, Q_2, and L_s, and C_S and C_P in Figure 7 constitute the first group of bucks, where Q_1 and Q_2 are collectively called P-arms. Moreover, Q_3, Q_4, L_P, and C_P form the second group of buck converters, among which Q_3 and Q_4 are collectively called the S-arms. The i_P current provides energy for the load, and the i_S current provides a reverse ripple current to cancel the ripple of the i_P current.

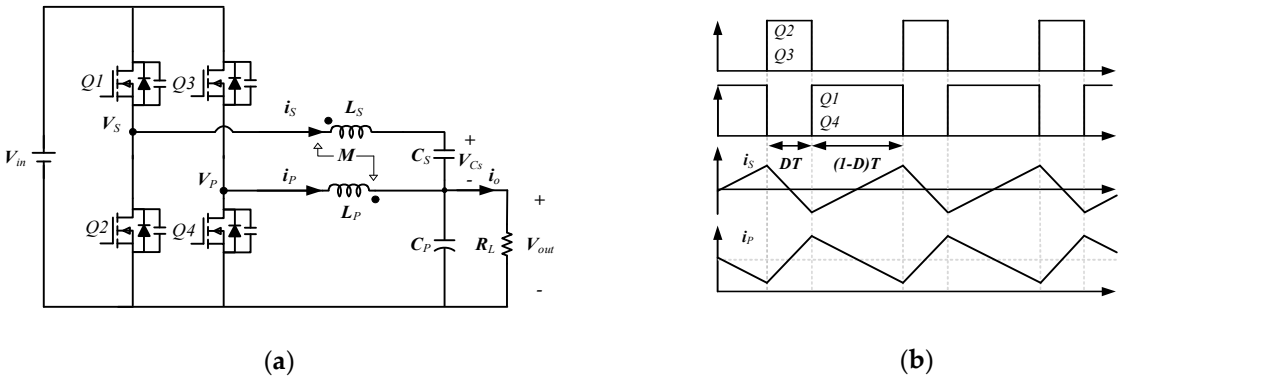


Figure 7. Stacked buck converter: (**a**) Circuit architecture diagram; (**b**) Operation sequence diagram.

Compared to the two architectures reviewed in Section 2, the stacked buck converter's main idea is not to use a fourth-order filter to suppress the output current ripple. Therefore, substantial capacitance and inductance values are not required to suppress the output current ripple well. Therefore, the stacked buck converter can use a smaller inductor and capacitance value to achieve the same current ripple suppression effect. In other words, the stacked buck converter essentially has better transient response performance.

The duty cycle of Q_3 as D_P is defined. Given that the inductance L_P satisfies the volt-second balance in the steady-state, $V_{out} = D_P V_{in}$ can be obtained from the second group of buck converters. $V_{out} + V_{Cs} = V_{in}(1 - D_P)$ can be obtained from the first group of buck converters. Moreover, we can deduce that $V_{Cs} = V_{in}(1 - 2D_P)$.

When Q_2 and Q_3 are turned on, the current change slopes of i_P and i_S are respectively expressed as follows:

$$\begin{aligned} \frac{di_P}{dt} &= \frac{L_P(V_P - V_{out}) + M(V_S - V_{Cs} - V_{out})}{{L_P}^2 - M^2} \\ &= \frac{L_P V_{in}(-D_P) + M V_{in}(D_P)}{(L_P + M)(L_P - M)}, \end{aligned} \tag{27}$$

$$\begin{aligned} \frac{di_S}{dt} &= \frac{M(V_P - V_{out}) + L_S(V_S - V_{Cs} - V_{out})}{{L_S}^2 - M^2} \\ &= \frac{M V_{in}(-D_P) + L_S V_{in}(D_P)}{(L_S + M)(L_S - M)}. \end{aligned} \tag{28}$$

When $L_P = L_S = L$, Equations (27) and (28) are added to obtain the following equation:

$$\begin{aligned} \frac{di_P}{dt} + \frac{di_S}{dt} &= \frac{V_P + V_S - 2V_{out} - V_{Cs}}{L - M} \\ &= \frac{V_{in} + 0 - 2D_P Vin - V_{in}(1 - 2D_P)}{L - M} \\ &= 0. \end{aligned} \tag{29}$$

Evidently, Equation (29) is zero and does not contain the variable of the duty. The preceding derivation indicates that the cascaded buck converter can eliminate current ripples under any duty cycle. The stacked buck converter's output current ripple elimination mechanism cancels the output current ripple by generating currents with opposite slopes from two sets of inductors. Such characteristics can ideally design the inductance value arbitrarily without affecting the output current ripple's cancellation effect. To achieve an ideal current ripple elimination effect, the voltages of C_S and C_P should approximate the ideal voltage source. However, the transient response of the converter, in this case will have a detrimental effect.

If V_{Cp} is set as an ideal voltage source, then V_{Cs} is a variable capacitor voltage. Accordingly, $V_P + V_S = V_{in}$ because the two arm switches are entirely complementary.

A review of Equation (29) indicates that if the slope of change of $i_P + i_S$ is desired to be positive, then the voltage of V_{Cs} should be less than $(1 - D_P)V_{in}$, which is below the steady-state value of the steady V_{Cs} voltage. That iss, when the C_S capacitance is low, the voltage of V_{Cs} is considerably susceptible to the i_S current, and the overall transient response of the converter is improved. However, this design concept will increase the ripple of V_{Cs} and reduce the effect of the current ripple elimination.

Compared with the fourth-order filter architecture, the stacked buck converter can use the upper or lower switches of the P and S arms to be turned on simultaneously to increase the transient response. Moreover, there is no need to deliberately reduce the capacitance of the C_S capacitor to sacrifice the current ripple elimination effect in exchange for the transient response speed. Review Equation (29) again, and substitute the V_P and V_S of Equation (29) into the input voltage V_{in}, representing that the upper bridge switches of the P- and S-arms are turned on. V_{Cp} and V_{Cs} are regarded as ideal voltage sources, and the rate of change of $i_P + i_S$ is as follows:

$$\frac{di_P}{dt} + \frac{di_S}{dt} = \frac{V_{in} + V_{in} - 2D_P Vin - V_{in}(1 - 2D_P)}{L - M}. \tag{30}$$

If V_P and V_S are substituted into the ground level, then the lower bridge switches representing the P- and S-arms are turned on. Moreover, V_{Cp} and V_{Cs} are regarded as ideal voltage sources, and the rate of change of $i_P + i_S$ is as follows:

$$\frac{di_P}{dt} + \frac{di_S}{dt} = \frac{0 + 0 - 2D_P Vin - V_{in}(1 - 2D_P)}{L - M}. \tag{31}$$

Equations (30) and (31) show that although V_{Cs} and V_{Cp} are constant voltage sources, the total inductor current change rate when the numerators of these equations are not zero can still be based on the control signal. Hence, $V_P = V_S = V_{in}$ or $V_P = V_S = 0$ to achieve the rising or falling slope. Moreover, the design of L and M can adjust the magnitude of the change slope. By simultaneously turning on the upper or lower switches of the two arms, the stacked buck converter can retain the current ripple elimination characteristics and meet transient response needs.

4. Boundary Limit Control Method

The description in Section 3 indicates that the stacked buck converter should be synchronized with the upper or lower bridge switches of the P- and S-arms to meet the transient response requirements.

To achieve this control interval, the literature [21] has indicated that adding an RC delay circuit to the feedback compensation output V_{EA} of the original complementary con-

troller can easily and simultaneously manufacture the upper and lower bridge switches of the P- and S-arms. The conduction period can improve the transient response. Figure 8a,b shows complementary and RC delay controllers, respectively. *Duty_P* is the driving signal of the P-arm upper bridge switch Q_3, and *Duty_S* is the driving signal of the S-arm upper bridge switch Q_1.

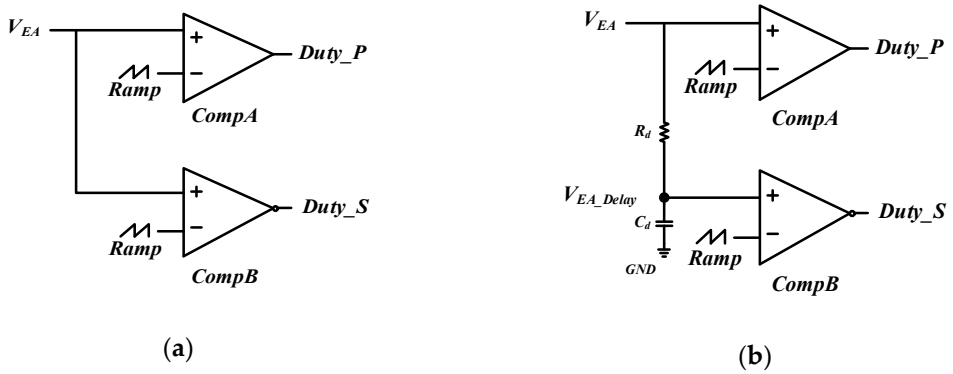


Figure 8. PWM controller: (**a**) Complementary type; (**b**) RC delay type.

Figure 9 illustrates the operation sequence diagram of the RC delay type controller. When the output load increases, the compensator output V_{EA} changes from steady-state operation to positive saturation V_{EA_sat}, which is the operation sequence diagram of V_{EA} relative to PWM in this changing interval. Figure 9 can be divided into three regions. Region I is the steady-state operation area, region II is the transient operation area, and region III is the saturation area. In region I, V_{EA} and V_{EA_Delay} can be regarded as the same signal, and *Duty_P* and *Duty_S* can be regarded as ideal complementary signals because the system reaches a steady-state. The output current ripple elimination mechanism is often operational. In region II, the output loading is increasing. The V_{EA} voltage begins to increase owing to the feedback system. V_{EA} and V_{EA_Delay} can no longer be regarded as the same signal because of the RC delay circuit, and the voltage amplitude V_{EA} is greater than V_{EA_Delay}. Therefore, *Duty_P* and *Duty_S* in region II have a duty overlap area, and the length of this area depends on the voltage difference between V_{EA} and V_{EA_Delay}. Duty overlap enables the converter to increase transient response. However, given that the system output voltage cannot stabilize immediately, the V_{EA} and V_{EA_Delay} voltages reach positive saturation and enter region III. In this region, the overlapping area of *Duty_P* and *Duty_S* disappears, returning to the general complementary operation, which significantly reduces the rising slope of the overall output current. However, the output load should receive energy at this time. Such an operation behavior further prolongs the time required for the output voltage to stabilize, and the depth of the output voltage undershoot increases. Therefore, the RC delay type control method cannot effectively adjust the converter's output when the compensator reaches saturation.

Given the lack of RC delay control, this study proposes a boundary limit control method suitable for stacked buck converters. Apart from accelerating the transient response, the boundary limit control method is not limited by the saturation of the compensator. Figure 10 shows a schematic of the boundary limit control method. The control principle aims to set the upper and lower limits of V_{EA}, and the limit value is fixed at the steady-state V_{EA} and take a settable boundary to generate a feedback compensation output V_{EA_Limit}.

Figure 11 shows the switch and control signal under the boundary limit control method. In region I, V_{EA} and V_{EA_Limit} maintain the same voltage because the system reaches a steady-state, and *Duty_P* and *Duty_S* maintain complementary operations. In region II, V_{EA} increases owing to an increase in load. When V_{EA} deviates from the steady-state V_{EA} value and the set limit boundary, the V_{EA} voltage is maintained, and V_{EA_Limit} is limited by the upper and lower limits. The result is the voltage difference between V_{EA} and V_{EA_Limit}, thereby making the duty of the P- and S-arm switches have an overlapping

interval. In region III, although V_{EA} reaches positive saturation, the P- and S-arm switch signals maintain an overlapping interval because V_{EA_Limit} is limited, thereby continuously increasing the transient response of the system.

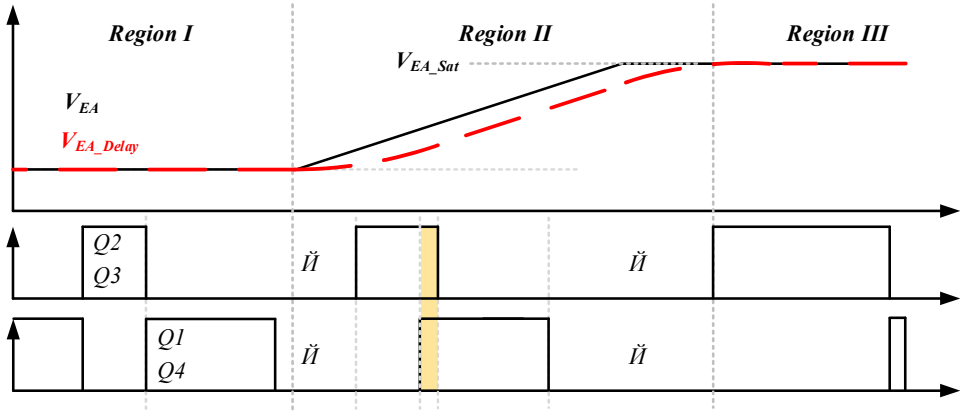


Figure 9. PWM signal of the RC delay controller in the V_{EA} steady-, transient, and saturation states.

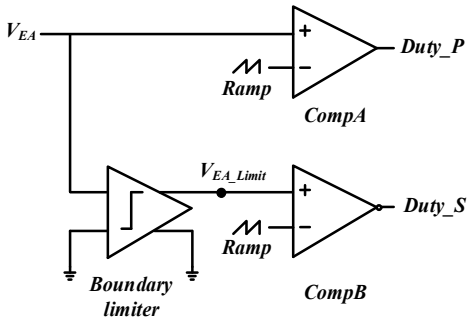


Figure 10. Schematic of the boundary limit control method.

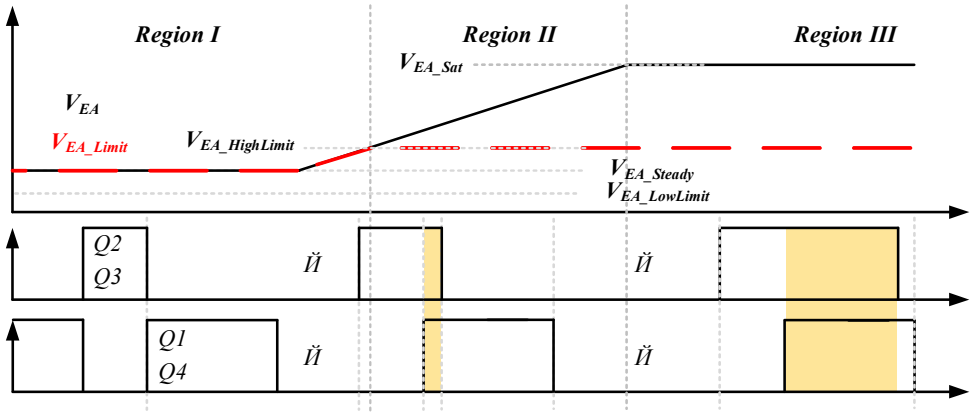


Figure 11. PWM signal of the boundary limit controller in the V_{EA} steady-, transient, and saturation states.

Figures 12 and 13 show the simulation results of the complementary and boundary limit controllers for the transient response. The system architecture diagram, circuit parameters, and compensator parameters are shown in Table 1, and Equation (56), respectively. The load resistance switches from R_L = 2.5 Meg Ω to R_L = 2.5 Ω at t = 70 mS, and switches from R_L = 2.5 Ω to 2.5 Meg Ω again at t = 120 mS. Figures 12 and 13 show that both control methods can achieve the effect of eliminating current ripples in the steady-state. Regarding the performance of the overshoot and undershoot of the output voltage, the boundary limit control method was superior to the complementary control method. Using

the boundary limit control method to replace the complementary control method, the overshoot performance of the output voltage decreased from 417 mV to 361 mV, and the undershoot performance decreased from 370 mV to 324 mV.

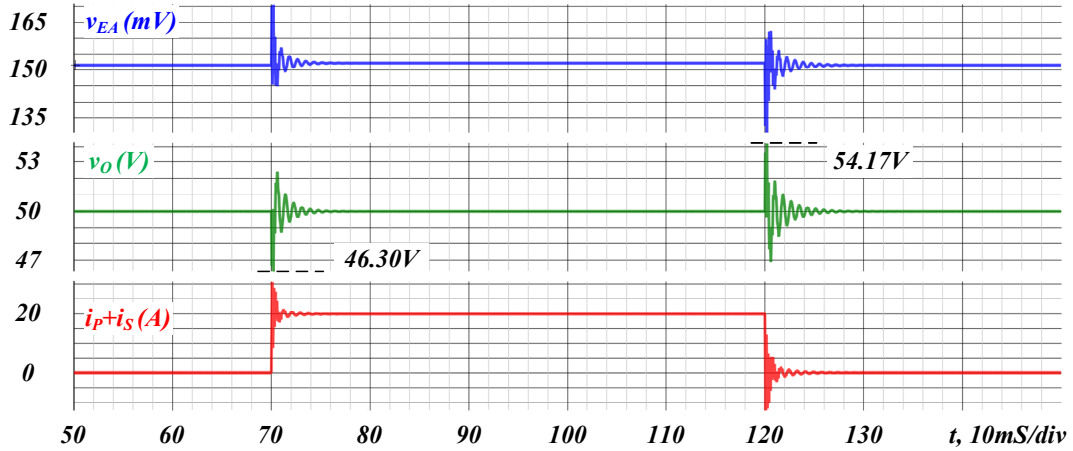


Figure 12. Simulation result of the transient response of the stacked buck converter with the complementary control method.

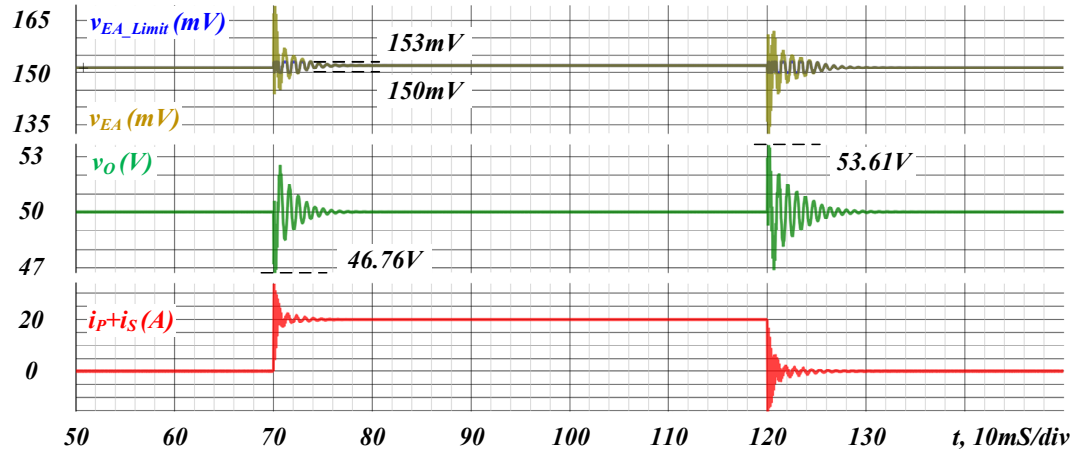


Figure 13. Simulation result of the transient response of the stacked buck converter with the boundary limit control method.

Table 1. Circuit parameters.

Symbols	Parameter Names	Specifications
f_{sw}	Switching frequency	100 kHz
V_{in}	Input voltage	330 V
V_{out}	Output voltage	48 V
L	Self-inductance	40 µH
M	Mutual inductance	30 µH
C_S	Blocking capacitance	200 µF
ESR_{Cs}	Blocking capacitance series resistance	30 mΩ
C_P	Output capacitance	150 µF
ESR_{Cp}	Output capacitance series resistance	10 mΩ
R_L	Load Resistance	2.5 Ω
R_{Sseq}	S-arm loop series equivalent impedance	10 mΩ
R_{Speq}	P-arm loop series equivalent impedance	10 mΩ
C_{oss}	Parasitic capacitance of the Q_1 to Q_4 switches	300 pF

5. Dead Time Modulation Method for Low Output Ripple

The output current ripple cancellation effect of the stacked buck converter in the existing system is affected by the actual dead time between the lower bridge switches. Hence, a necessary step is to understand the origin of the steady-state voltage value on the C_S capacitor and the relationship between the voltage on the C_S capacitor and the cancellation effect of the output current ripple.

Figure 14 shows the equivalent circuit diagram redrawn by converting the coupled inductor in Figure 7a into a T-type model and unifying the symbols with $L_S = L_P = L$.

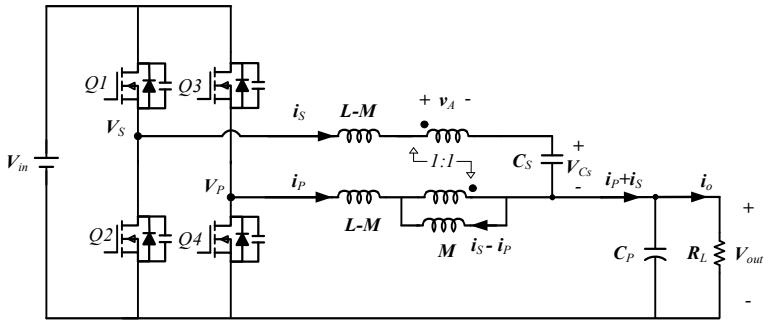


Figure 14. Stacked buck converter with coupled inductor equivalent T model.

To immediately understand and analyze the impact caused by dead time, the discussion of the circuit mode is limited to the idea that the output load condition is sufficiently large to make the current of i_P constantly above zero.

To simplify the analysis, V_{out} and V_{Cs} can be regarded as fixed DC voltages by assuming that the capacitances of C_P and C_S are sufficiently large. In the dead time, the inductor L-M's current change is small to be regarded as a constant current source. The switch's parasitic capacitance C_{oss} is fixed and does not change with the voltage across it. Moreover, the turn-on voltage drop of the body diode of the switch is disregarded as 0 V.

First, the steady-state voltage value of V_{Cs} is derived with an ideal stacked buck converter. Given that the switching signals are entirely complementary, the node voltages V_P and V_S have only two states: State 1, $V_S = V_{in}$, $V_P = 0$; and State 2, $V_S = 0$, $V_P = V_{in}$. Solving V_{Cs} for these two states, the derivation process is as follows.

State 1, $V_S = V_{in}$, $V_P = 0$, according to KCL and KVL, the equation can be written as follows:

$$i_S(s) = \frac{s^{-1}(V_{in} - v_A - V_{Cs} - V_{out})}{s(L-M)}, \tag{32}$$

$$i_P(s) = \frac{s^{-1}(0 + v_A - V_{out})}{s(L-M)}, \tag{33}$$

$$v_A(s) = [i_S(s) - i_P(s)]M. \tag{34}$$

Substituting Equations (32) and (33) into Equation (34) can solve for v_A, and rename v_A in state 1 to v_{A1}. The resulting equation is as follows:

$$v_{A1}(s) = \frac{s^{-1}(V_{in} - V_{Cs})}{\frac{L-M}{M} + 2}. \tag{35}$$

State 2, $V_S = 0$, $V_P = V_{in}$, according to KCL and KVL, the equation can be written as follows:

$$i_S(s) = \frac{s^{-1}(0 - v_A - V_{Cs} - V_{out})}{s(L-M)}, \tag{36}$$

$$i_P(s) = \frac{s^{-1}(V_{in} + v_A - V_{out})}{s(L-M)}, \tag{37}$$

$$v_A(s) = [i_S(s) - i_P(s)]M. \tag{38}$$

Substituting Equations (36) and (37) into Equation (38) can solve for v_A, and rename v_A in state 2 to v_{A2}. The resulting equation is as follows:

$$v_{A2}(s) = \frac{s^{-1}(-V_{in} - V_{Cs})}{\frac{L-M}{M} + 2}. \tag{39}$$

The steady-state indicates that the inductance M must satisfy the volt-second balance to write Equation (40), where V_{A1} and V_{A2} are the DC voltage levels obtained by the inverse Laplace conversion of v_{A1} and v_{A2}, respectively, as follows:

$$V_{A1}(1 - D_P) + V_{A2}D_P = 0. \tag{40}$$

Substituting Equations (35) and (39) into Equation (40) after the inverse Laplace transformation, we obtain the following equation:

$$\frac{1}{\frac{L-M}{M} + 2}[(V_{in} - V_{Cs})(1 - D_P) + (-V_{in} - V_{Cs})D_P] = 0. \tag{41}$$

Thereafter, solving Equation (41) can obtain V_{Cs} as follows:

$$V_{A1}(1 - D_P) + V_{A2}D_P = 0. \tag{42}$$

A review of Equation (29) indicates that when $V_P + V_S - V_{Cs} = 2D_PV_{in}$ must be satisfied (i.e., when $V_{Cs} = (1 - 2D_P)V_{in}$), the slope of $i_P + i_S$ will be zero. In an ideal stacked buck converter, the relationship of Equation (29) is satisfied because the switching signals are completely complimentary. Hence, the output current ripple elimination behavior can be ideally achieved. However, in practical applications, the upper and lower bridge switches inevitably contain a dead time. Thus, the stacked buck converter's current ripple elimination effect should be re-discussed.

Figure 15 shows an operation sequence diagram of a stacked buck converter with conventional dead time. Dead time is fixed, and four switches are turned off simultaneously. The operation sequence diagram in Figure 15 can be divided into three sections: switch conduction section (t_0~t_1, t_2~t_3) and two different dead times (t_1~t_2, t_3~t_{0+T}).

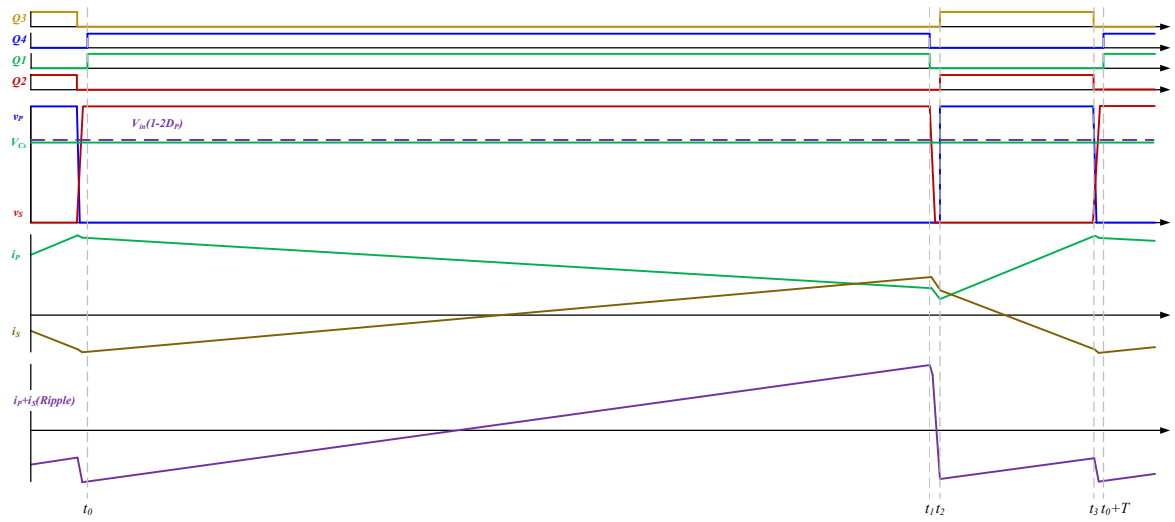


Figure 15. Operation sequence diagram of a stacked buck converter with conventional dead time.

The action sequence diagram shows that the ripple slope of $i_P + i_S$ rises in the conduction interval of the two switches. In the two switch dead time intervals, the ripple slope

change phenomenon of $i_P + i_S$ is different, but both make $i_P + i_S$ present an equivalent falling slope. Moreover, the voltage amplitude of V_{Cs} is slightly lower than $(1 - 2D_P)V_{in}$.

The following discussion focuses on the three intervals to explain the behavior of the current ripple slope change of $i_P + i_S$. To make the waveform more convenient for discussion, the two dead time intervals of t_1~t_2 and t_3~t_{0+T} in Figure 15 are enlarged, leaving the V_P and V_S node voltage waveforms v_P and v_S, which are redrawn as Figure 16.

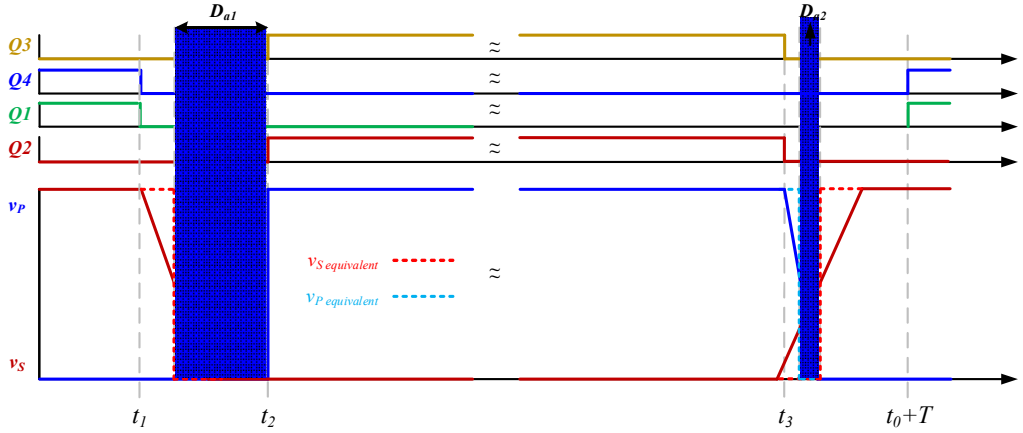


Figure 16. Operation sequence diagram of a stacked buck converter with conventional dead time (zoom in).

First, we discuss the dead time interval (t_1~t_2).

When $t = t_1$, all switches are off. Given that $i_P > 0$, the current will automatically flow through the body diode of Q_4 after switch Q_4 is turned off. The v_P voltage is maintained at 0 V until Q_3 is turned on at $t = t_2$ and the v_P voltage increases vertically from 0V to V_{in}. Given that $i_S > 0$, after Q_1 is turned off, the i_S current charges and discharges the C_{oss} of Q_1 and Q_2. The initial value of the current is the peak value of the i_S current. When the v_S voltage decreases to 0 V, the body diode of Q_2 turns on, clamping v_S to 0 V. When $t = t_1$, Q_2 turns on and Vs continues to maintain 0 V.

Given that the current of *is* in the dead time is regarded as a fixed value, the voltage of v_S decreases linearly. The v_S discharge falling interval is taken as half of its falling time, and the equivalent v_S waveform $v_{S\ equivalent}$ can be drawn. From the equivalent v_S waveform, there is evidently a duty cycle D_{a1} between $t = t_1$ and $t = t_2$, and its equivalent v_P and v_S are 0 V.

From Equation (29), the slope of $i_P + i_S$ is controlled by $v_P + v_S - 2V_{out} - v_{Cs}$. When v_{Cs} is equal to $(1 - 2D_P)V_{in}$, and $v_P + v_S$ is V_{in}, the current ripple offset can be achieved. However, in the dead time $t = t_1$~t_2 interval, except that v_{Cs} is slightly lower than $(1 - 2D_P)V_{in}$, and $v_P + v_S$ is smaller than V_{in}. Given that $v_P + v_S - 2V_{out} - v_{Cs} < 0$, the change slope of $i_P + i_S$ during the entire dead time interval is negative.

Second, we discuss the dead time interval (t_3~t_{0+T}).

When $t = t_3$, all switches are off. Given that $i_P > 0$, after the switch, Q_3 is turned off, the peak current of i_P charges and discharges the C_{oss} of Q_3 and Q_4. When the v_P voltage drops to 0 V, the body diode of Q_4 turns on and clamps v_P to 0 V. When $t = t_{0+T}$, Q_4 turns on, and v_P continues to maintain 0 V.

Note that the peak direct current of i_P will change with load conditions. Thus, v_P's discharge slope will become rapid as load increases.

Given that $i_S < 0$ after Q_2 is turned off, the peak current of *is* charges and discharges C_{oss} of Q_1 and Q_2. When the v_S voltage rises to V_{in}, the body diode of Q_1 is turned on, clamping v_S to V_{in}; and when $t = t_{0+T}$, Q_1 is turned on and v_S continues to maintain V_{in}. Moreover, given that the average current of i_S is zero in the steady-state, the positive and negative peak currents of i_S are equal in magnitude. Therefore, the time for the v_S voltage in the dead time $t = t_3$~t_{0+T} to rise from 0 V to V_{in} is the same as the time for the v_S voltage to fall from V_{in} to zero in the dead time $t = t_1$~t_2.

Given that the currents of i_P and i_S in the dead time are regarded as fixed values, v_S and v_P change voltages linearly. If half of the time of the voltage linear change of v_P and v_S, then the equivalent waveforms of v_S and v_P, $v_{S\ equivalent}$ and $v_{P\ equivalent}$ can be drawn. From the equivalent v_S and equivalent v_P waveforms, it can be observed that there is a duty period D_{a2} between time t_3 and t_{0+T}, and the equivalent v_P and v_S are both 0 V.

The slope of $i_P + i_S$ is controlled by $v_P + v_S - 2V_{out} - v_{Cs}$. When v_{CS} is equal to $(1 - 2D_P)V_{in}$ and $v_P + v_S$ is V_{in}, the current ripple cancellation can be achieved. However, in the dead time $t = t_3 \sim t_{0+T}$, except that v_{Cs} is slightly lower than $(1 - 2D_P)V_{in}$, $v_P + v_S = V_{in}$ after the body diodes of Q_1 and Q_4 are turned on. Therefore, in the dead time interval's front and back zone, given that $v_P + v_S - 2V_{out} - v_{Cs} > 0$, the slope of change of i_P+i_S rises slightly. However, the equivalent v_P and v_S waveforms shows a D_{a2} equivalent duty cycle, and the v_P and v_S are both 0 V. The resulting falling slope of $i_P + i_S$ is considerably larger than the other slight rising slopes. Hence, the overall i_P+i_S change continues to decrease in the dead time interval from $t = t_3 \sim t_{0+T}$.

Lastly, we discuss the switch conduction interval ($t_0 \sim t_1$, $t_2 \sim t_3$):

The previous two dead time intervals show equivalent duty cycles D_{a1} and D_{a2}. Hence, v_P and v_S are both 0 V. We define a new equivalent duty cycle D_A, where $D_A = D_{a1}$+D_{a2}. Given the converter's new state, the previous derivation of v_A and V_{Cs} should be imitated and V_{Cs} voltage amplitude under the D_A duty cycle should be derived. From Figure 14, we can deduce that the circuit equation of the circuit state under the D_A duty cycle is as follows.

State 3, $V_S = 0$, $V_P = 0$, according to KCL and KVL, the equations can be written as follows:

$$i_S(s) = \frac{s^{-1}(0 - v_A - V_{Cs} - V_{out})}{s(L - M)}, \tag{43}$$

$$i_P(s) = \frac{s^{-1}(0 + v_A - V_{out})}{s(L - M)}, \tag{44}$$

$$v_A(s) = [i_S(s) - i_P(s)]M. \tag{45}$$

Substituting Equations (43) and (44) into Equation (45) can solve for v_A, and rename v_A in state 3 to v_{A3} as follows:

$$v_{A3}(s) = \frac{s^{-1}(-V_{Cs})}{\frac{L-M}{M} + 2}. \tag{46}$$

According to the steady-state, the volt-second balance of the inductance M can be written as Equation (47), where V_{A1}, V_{A2}, and V_{A3} are the DC voltage levels obtained by the inverse Laplace transformation of v_{A1}, v_{A2}, and v_{A3}, respectively:

$$V_{A1}(1 - D_P - D_A) + V_{A2}D_P + V_{A3}D_A = 0. \tag{47}$$

Substituting Equations (35) and (39) into Equation (40) after the inverse Laplace transformation can be obtained as follows:

$$\frac{1}{\frac{L-M}{M} + 2}[(V_{in} - V_{Cs})(1 - D_P - D_A) + (-V_{in} - V_{Cs})D_P + (-V_{Cs})D_A] = 0. \tag{48}$$

Thereafter, solving (48) can obtain the modified equation of V_{Cs} as follows:

$$V_{Cs} = (1 - 2D_P - D_A)V_{in}. \tag{49}$$

From Equation (49), when $D_A > 0$, V_{Cs} will be lower than $(1 - 2D_P)V_{in}$. Although in the conduction interval ($t_0 \sim t_1$, $t_2 \sim t_3$), $v_P + v_S = V_{in}$, Equation (29) still cannot be established. Hence, the slope of $i_P + i_S$ remains positive, and the ripple cannot be eliminated correctly.

This study proposes a dead time modulation method for low output ripple based on the preceding theoretical analysis. The modulation method is shown in Figure 17. Changing the timing of the on and off of the Q_3 switch can achieve the effect of low output ripple.

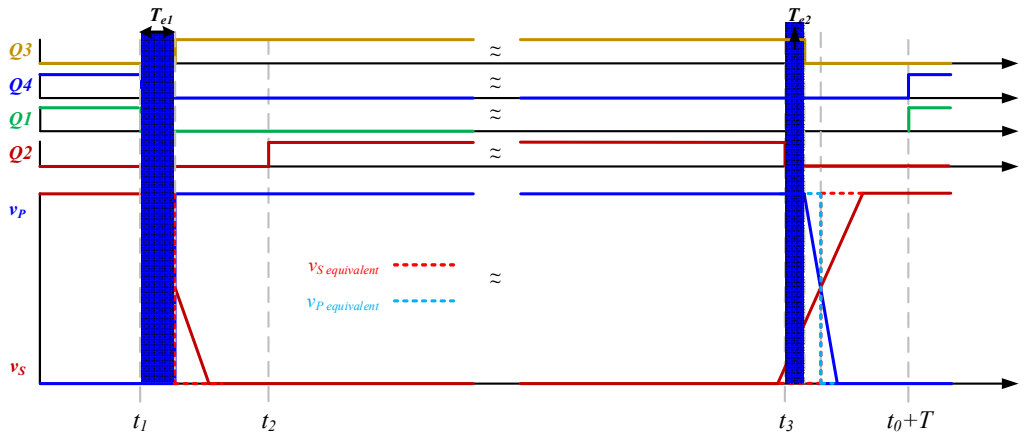


Figure 17. Operation sequence diagram of a stacked buck converter with low output ripple dead time modulation (zoom in).

The dead time modulation method for low output ripple aims to adjust the equivalent v_P and v_S waveforms to complement each other. Therefore, the Q_3 switch is turned on in advance and turned off later. Figure 17 shows that the equivalent v_P and v_S can be completely complementary through the dead time modulation method.

The minimum switching dead time (t_2-t_1, t_3~t_{0+T}) of the remaining switches and the time of T_{e1} and T_{e2} can be obtained through the following design steps.

Step 1, design the minimum switch dead time.

The dead time t_1~t_2 and t_3~t_{0+T} interval must be sufficiently long to enable the completion of the voltage transition of v_P and v_S in the dead time. Hence, the minimum switching dead time must be longer than the maximum voltage transition time of v_P and v_S. The longest transition time occurs when the S-arm switch is turned off, and the time required for the S-arm C_{oss} capacitor to charge and discharge through the peak current of i_S. The peak current of i_S, I_{S_pk}, can be derived from the V_{A1} obtained by the inverse Laplace transformation Equation (35), the ideal V_{Cs} in Equation (42), and duty cycle D_P:

$$I_{S\_pk} = \frac{(V_{in} - V_{A1} - V_{Cs} - V_{out})(1 - D_P)T_S}{2(L - M)}, \tag{50}$$

where T_s is the switching period.

The voltage waveform conversion time of v_S can be derived as follows:

$$T_{S\_tran} = \frac{2C_{oss} \cdot V_{in}}{I_{S\_PK}} \tag{51}$$

Therefore, the minimum switching dead time must be designed to be longer than T_{S_tran}.

Step 2, design the trigger time of T_{e1}:

Figure 17 shows that the time of T_{e1} is half of T_{S_tran}. The time of T_{e1} will not change with the output load and is a fixed value. It is written as an equation as follows:

$$T_{e1} = \frac{T_{S\_tran}}{2}. \tag{52}$$

Step 3, design the T_{e2} delay closing time:

Figure 17 shows that the time of T_{e2} is jointly determined by T_{S_tran} and the time when v_P transition from V_{in} to 0 V. When Q_3 is off, the peak current of i_P charges and discharges

the C_{oss} of the upper and lower bridge switches of the P-arm. Thus, the transition time of the v_P voltage is as follows:

$$T_{P\_tran} = \frac{2C_{oss} \cdot V_{in}}{I_{P\_PK}}, \tag{53}$$

where I_{P_PK} is the output load current I_O plus I_{S_PK}, and its current value changes with load conditions.

Thereafter, the delayed closing time T_{e2} is as follows:

$$T_{e2} = \frac{T_{S\_tran} - T_{P\_tran}}{2}. \tag{54}$$

Figures 18 and 19 show the simulation results of the output current ripple of the stacked buck converter under the conventional dead time and low output ripple dead time modulation. The system architecture diagram and system parameters are shown in Figure 27 and Table 1, respectively. Moreover, R_L = 10 Ω, and the dead time is set to 100 nS, T_{e1} = 32.67 nS, and T_{e2} = 20.34 nS. Figures 18 and 19 show that with the conventional dead time simulation results, the peak-to-peak value of the output current ripple is 2.4 A and the RMS value of the current ripple is 745 mA. Given that simulation results of the low output ripple dead time modulation, the peak-to-peak output current ripple decreases to 443.53 mA, and the RMS value of the current ripple is 15.78 mA. Note that the dead time modulation method of the low ripple output can significantly reduce the amount of current ripple. The result is consistent with the theoretical analysis.

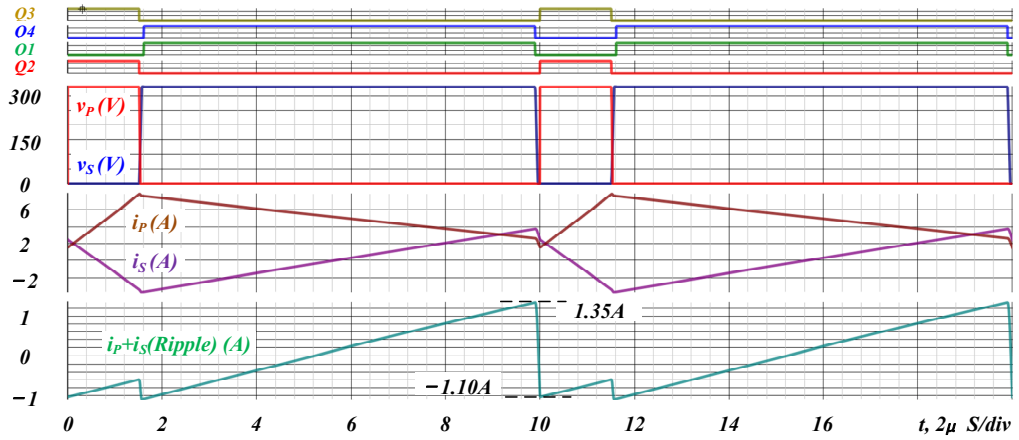


Figure 18. Simulation results of the output current ripple of a stacked buck converter with conventional dead time.

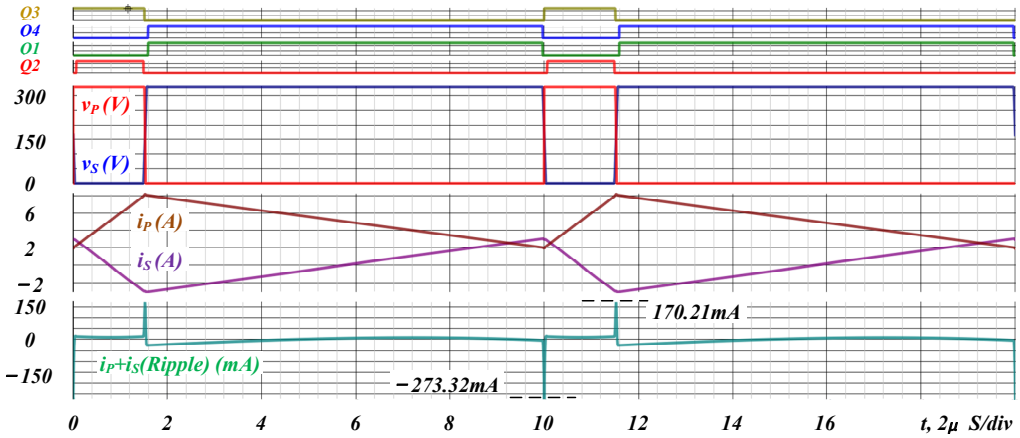


Figure 19. Simulation results of the output current ripple of a stacked buck converter with low output ripple dead time modulation.

6. Small-Signal Model and Compensation Design

The small-signal model of the independent inductor cascaded buck converter has been proposed in the literature [22]. Its small-signal model is extended to a coupled-inductor stacked buck converter, as shown in Figure 20. In particular, R_{Sseq} and R_{Speq} are the total series resistance on the series path, and the resistance value is the sum of the on-resistance of the power switch and resistance of the inductor winding. Furthermore, ESR_{CS} and ESR_{CP} are the equivalent series resistances of the C_S and C_P capacitors, respectively.

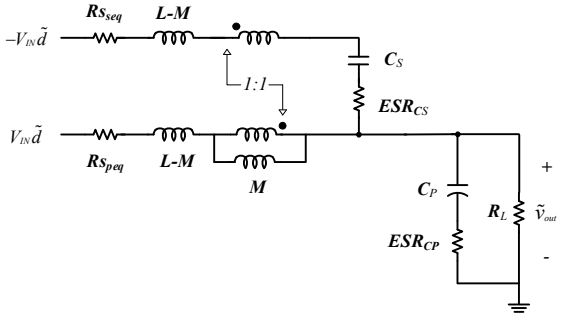


Figure 20. The small-signal model of a stacked buck converter in the form of coupled inductance.

To verify the accuracy of the small-signal model and determine the disturbance transfer function G_{dv} of *duty* to v_{out} under different load conditions, the circuit parameters are shown in Table 1. R_L is substituted into 2.5 Meg Ω and 2.5 Ω. Using the actual circuit operation and small-signal model, we use the simulation software to run the individual G_{dv} Bode diagrams, respectively $G_{dv\_circuit}$ and G_{dv_model}, as shown in Figure 21. Moreover, Figure 21 shows that $G_{dv\_circuit}$ and G_{dv_model} are consistent with each other, which proves the correctness of the small-signal model. Moreover, the worst case is when RL = 2.5 Meg Ω. Therefore, the compensator should be designed under the converter's no-load condition. Given that $G_{dv\_circuit}$ is consistent with G_{dv_model}, the following articles will use G_{dv} notation to represent the disturbance transfer function of duty to v_{out}, where $G_{dv} = G_{dv\_model} = G_{dv\_circuit}$.

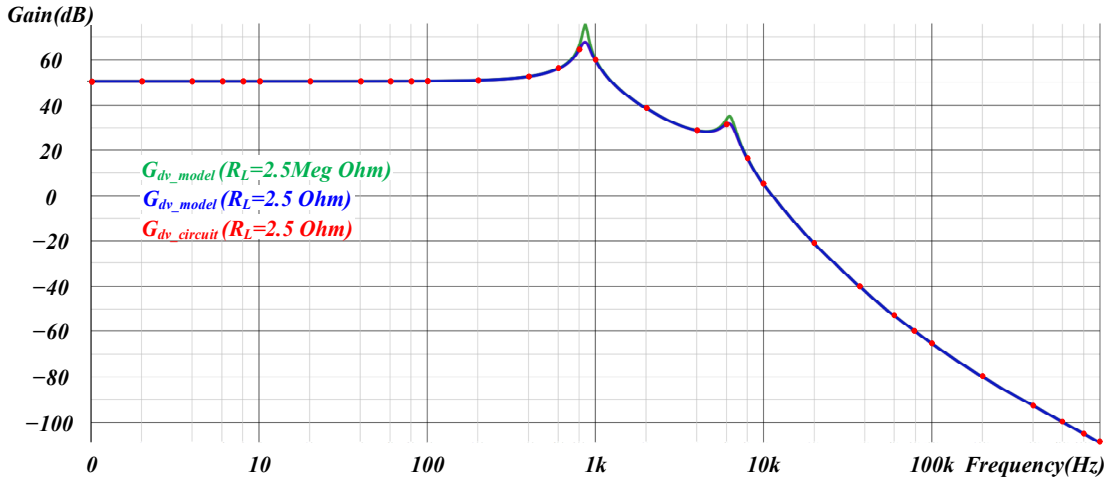


Figure 21. Bode plot of the G_{dv} transfer function of the small-signal model and the actual circuit operation of the cascaded buck converter in the form of coupled inductance.

When considering the use of boundary limit control, the stacked buck converter's small-signal model within the boundary-limited interval should be discussed. Given that the S-arm's duty disturbance in the boundary-limited interval is 0, the small-signal model in the boundary control interval can ground the S-arm's duty disturbance in Figure 20.

This result becomes the small-signal model of the stacked buck converter of the coupled inductance forms in the boundary limit interval. The model is shown in Figure 22.

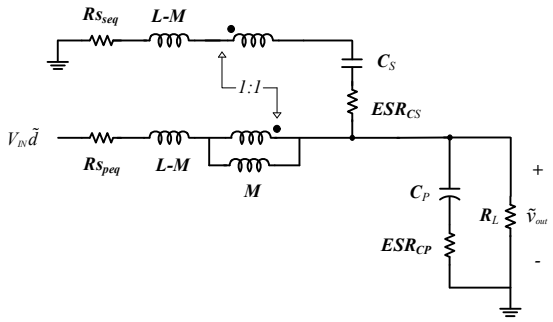


Figure 22. The small-signal model of a stacked buck converter in the form of coupled inductance within the boundary-limited interval.

Substitute the R_L of Figure 22 into 2.5 Meg Ω, plot the disturbance transfer function G_{dv_bd} of duty to v_{out} in the boundary control interval, and place it in Figure 23 together with the G_{dv} in Figure 21 for comparison. Figure 23 shows that the Bode plots of G_{dv} and G_{dv_bd} are extremely different regardless of the changes in gain and phase. Such characteristics will make it challenging to design the compensator with one compensator while satisfying the two closed loops' high-frequency bandwidth and stability.

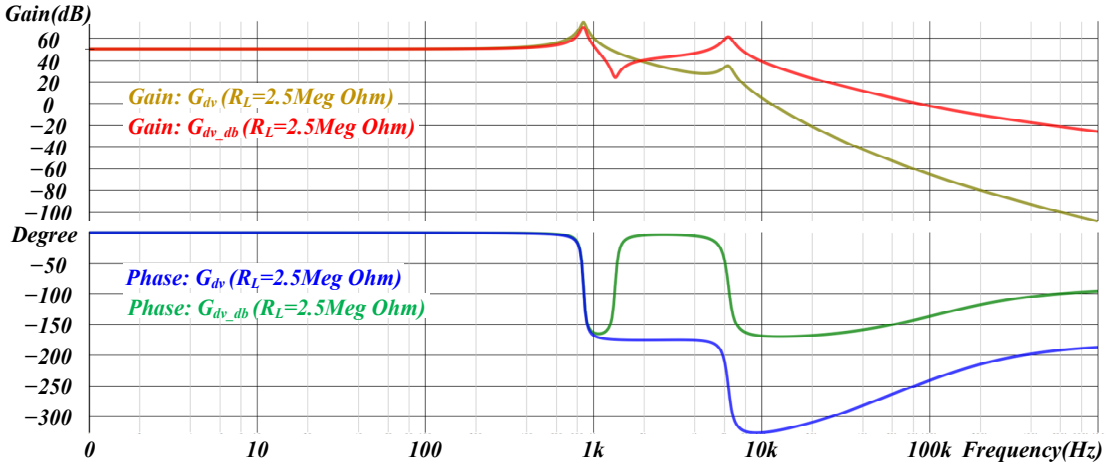


Figure 23. Bode plots of G_{dv} and G_{dv_bd}.

If the compensator's design aims to satisfy G_{dv} and G_{dv_bd}, then the easiest method is to reduce the closed-loop bandwidth. Therefore, the first compensator example's design parameters are shown in Equation (55), using single-pole compensation. Figure 24 shows the closed-loop gain under the first type of compensator, where $T_v = G_{dv}C_{ompType1}$ and $T_{v\_db} = G_{dv\_bd}C_{ompType1}$. Note that T_v and T_{v_bd} are stable and contain sufficient gain and phase margins. However, the closed-loop bandwidth is extremely narrow.

$$Comp_{Type1}(s) = \frac{2\pi \cdot 10}{330}\frac{1}{s}. \tag{55}$$

As the boundary control mode will eventually return to the ordinary operation mode, and G_{dv} is used as the basis for the final system stability, the second type of compensator design concept aims to design only for G_{dv} and disregard the stability of G_{dv_bd}. The design parameters of the second type of compensator are shown in Equation (56). Figure 25 shows the closed-loop gain using the second type of compensator, where $T_v = G_{dv}C_{ompType2}$

and $T_{v\_db} = G_{dv\_bd}C_{ompType2}$. Note that only the closed-loop gain of G_{dv} is stable, while the closed-loop gain of G_{dv_bd} has insufficient GM and PM in two places. Although the closed-loop bandwidth of G_{dv} is increased, the system has unstable factors in the boundary limit control mode.

$$Comp_{Type2}(s) = \frac{\left(1+\frac{s}{2\pi\cdot 800}\right)\left(1+\frac{s}{2\pi\cdot 800}\right)}{\left(1+\frac{s}{2\pi\cdot 5}\right)\left(1+\frac{s}{2\pi\cdot 14k}\right)\left(1+\frac{s}{2\pi\cdot 16k}\right)}. \quad (56)$$

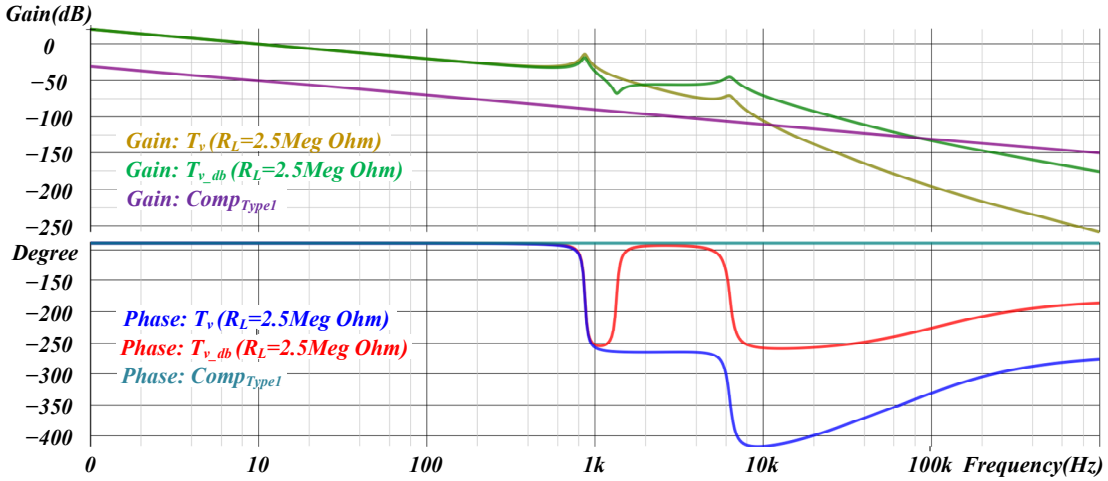


Figure 24. Bode plot of the closed-loop transfer function using the first compensator.

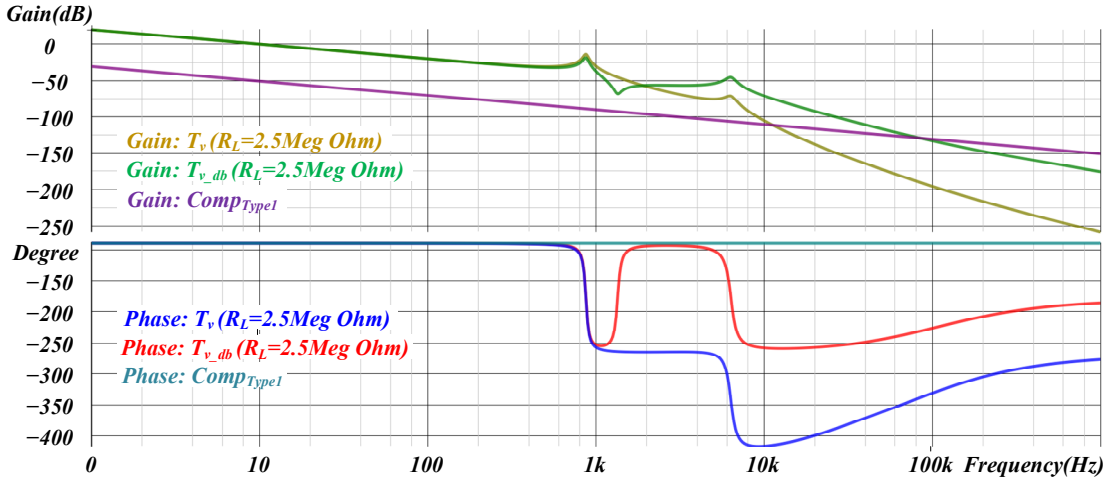


Figure 25. Bode plot of the closed-loop transfer function using the second compensator.

Figure 26 compares the simulation results of the system transient response of the first and second compensators. The load resistance is switched from R_L = 2.5 Meg Ω to R_L = 2.5 Ω when R_L is t = 70 mS. When t = 120 mS, the load resistance is switched from R_L = 2.5 Ω to 2.5 Meg Ω again. Figure 26 shows that the transient response of the first type of compensator is considerably slow, the boundary limit mode is not triggered, and the system is stable but takes a long time to reach the steady-state. However, the transient response of the second type of compensator has a short recovery time. It triggers the boundary limit mode. Hence, the performance of undershoot and overshoot is better, the output voltage is stabilized for a short time, and the system returns to stability in the general operation mode. Figure 26 shows that with the second type of compensator, the system can eventually return to stability even though T_{v_db} has unstable factors.

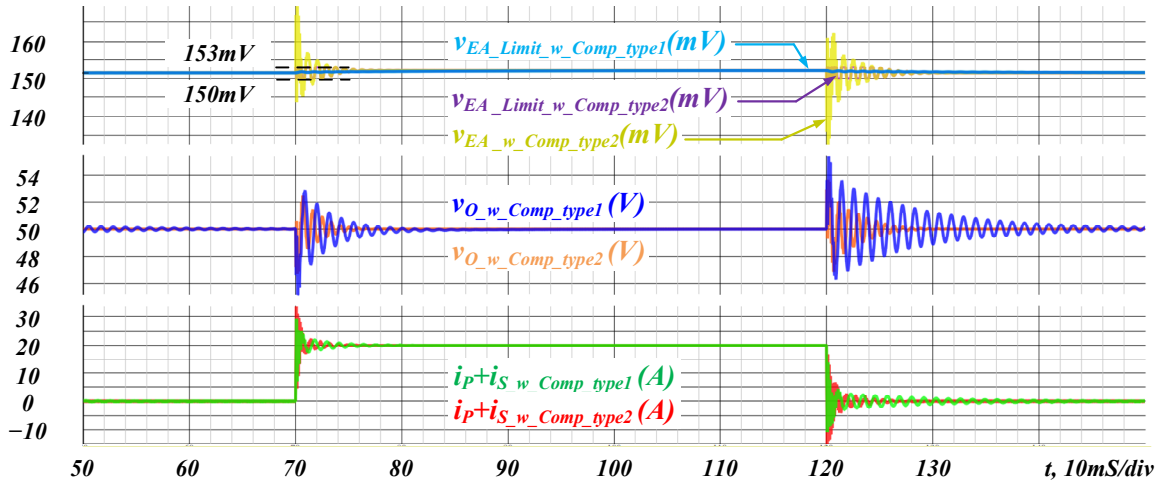


Figure 26. Comparison of the simulation results of the system transient response of the first and second compensators.

7. Implementation Verification Results

To verify the effectiveness of the low ripple dead time modulation method proposed in this study, a prototype circuit is actually made for verification. Figure 27 shows the implementation circuit diagram. Table 1 presents the implementation circuit parameters. The dead time modulation parameters are full load as an example, using the modulation parameters when R_L = 2.5 Ohm. The relevant parameters are shown in Table 2.

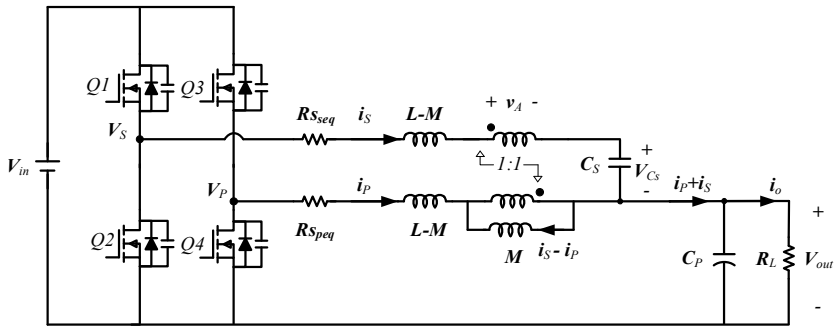


Figure 27. Implementation circuit diagram of a stacked buck converter in the form of coupled inductor.

Table 2. Dead time modulation parameters.

Symbols	Parameter Names	Specifications
$T_{dead\ time}$	Dead time	100 ns
T_{e1}	The time difference between Q_4 switch off and Q_3 switch on	32.67 ns
T_{e2}	The time difference between Q_2 switch off and Q_3 switch off	28.37 ns

Figure 28 shows the waveforms of v_P, v_S, i_P, and i_S, using the conventional dead time and low output ripple dead time modulation with R_L = 2.5 Ω. Figure 28a shows that using the conventional dead time stacked buck converter, the i_P and i_S current waveforms both show a steep falling slope in the dead time interval, and it is expected that the current ripple of i_P + i_S cannot be accurately cancellate. Moreover, Figure 28b shows that the stacked buck converter using the low output ripple dead time modulation, the current waveforms of i_P and i_S present a reverse slope in the dead time interval, and the current ripple of the entire switching cycle presents a complete triangle wave. It can be expected to accurately cancellate the current ripple of i_P + i_S.

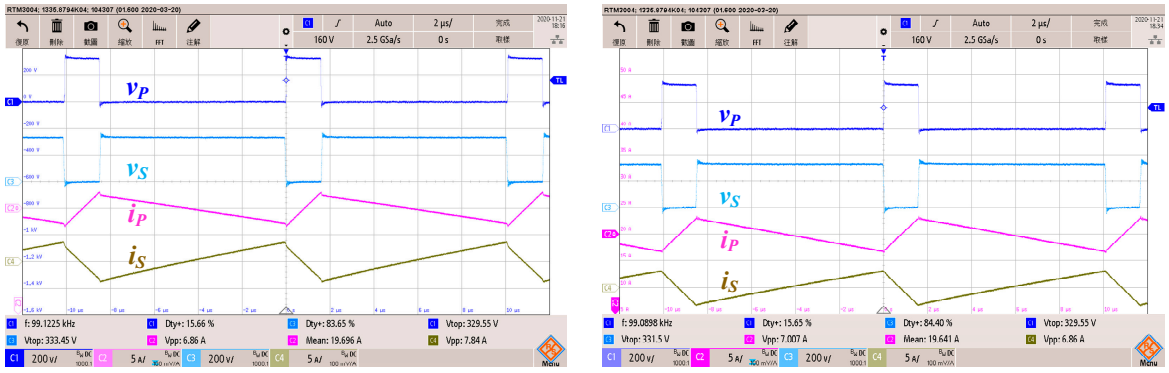


Figure 28. Measured waveforms of the switching node voltage and inductor current: (**a**) conventional dead time; (**b**) low output ripple dead time modulation. [scale v_P (Ch1): 200 V/div; i_P (Ch2): 5 A/div; v_S (Ch3): 200V/div; i_S (Ch4): 5A/div; time: 2 µs/div].

Figure 29 shows waveforms of v_P, v_S, $i_P + i_S(AC)$, and i_o, using the conventional dead time with R_L = 2.5 Ω. Figure 29 shows that using the conventional dead time stacked buck converter, in the dead time interval (t_1~t_2, t_3~t_{0+T}), because $v_P + v_S < Vin$, the current ripple of $i_P + i_S$ has a steep falling slope.

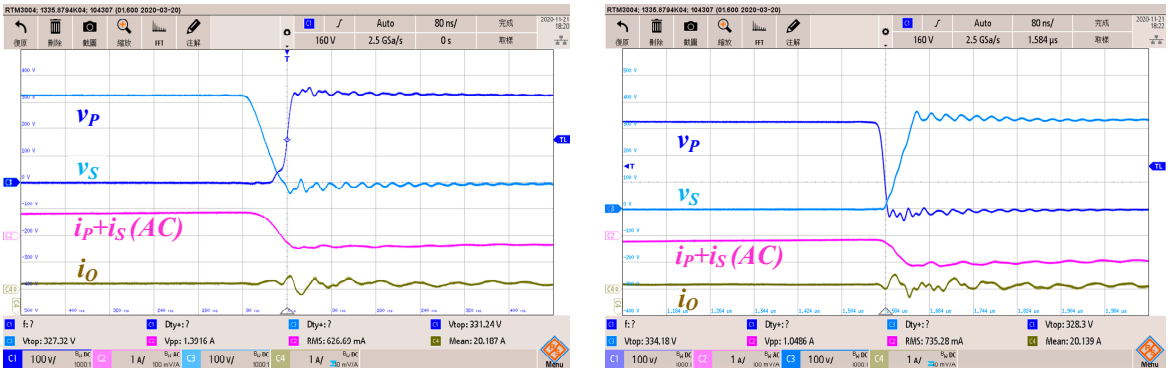
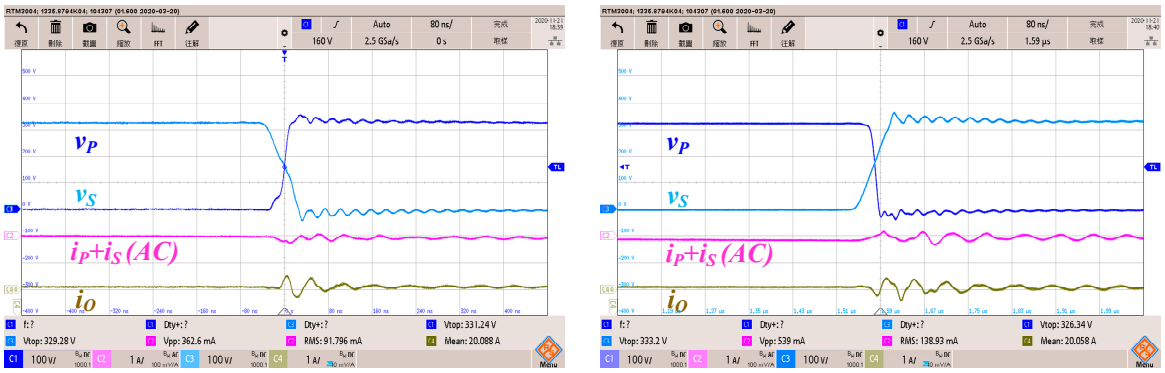


Figure 29. Measured waveforms of the switching node voltage, sum of inductor current ripple and output current using the conventional dead time: (**a**) dead time interval: t_1~t_2; (**b**) dead time interval: t_3~t_{0+T}. [scale v_P (Ch1): 200 V/div; $i_P + i_S$ (*AC*) (Ch2): 5 A/div; v_S (Ch3): 200V/div; i_O (Ch4): 1A/div; time: 80 ns/div].

Figure 30 shows waveforms of v_P, v_S, $i_P + i_S(AC)$, and i_o, using the low output ripple dead time modulation with R_L = 2.5 Ω. Figure 30 shows that using the low output ripple dead time modulation, in the dead time interval (t_1~t_2, t_3~t_{0+T}), since the equivalent voltage of the switching node voltage is complementary, the ripple of $i_P + i_S$ can be minimized. Because the switching node's voltage has switching noise, and the parasitic capacitance C_{oss} of the switch will change the capacitance value with the difference of the cross voltage, the calculated T_{e1} and T_{e2} are different from the time required on the existing system. Therefore, the current ripple elimination effect in practice is not as good as the simulation result. However, it can be seen from the actual measurement results that the ripple of $i_P + i_S$ has been greatly reduced, and the maximum peak to peak amount comes from the switching noise rather than the operation interval where v_P and v_S voltage overlap.

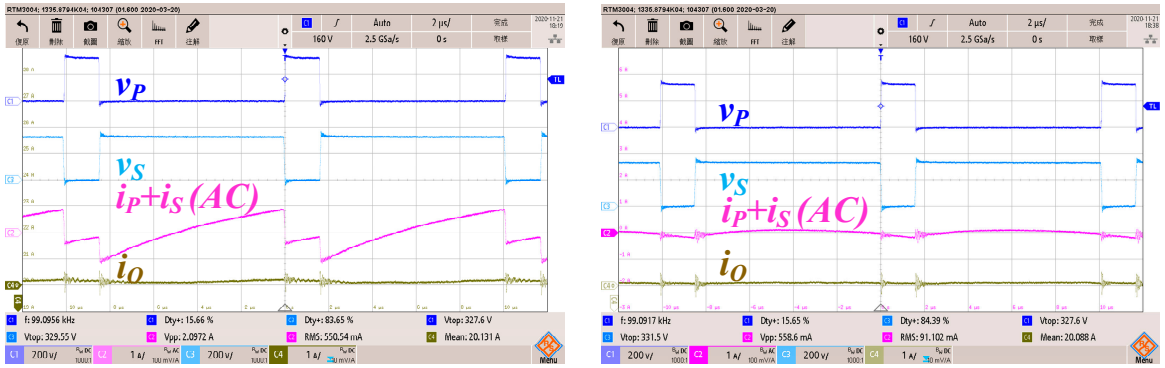
Figure 31 shows the waveforms of v_P, v_S, i_P, and i_S, using the conventional dead time and low output ripple dead time modulation with R_L = 2.5 Ω. Figure 31a shows that using the conventional dead time stacked buck converter, the peak-to-peak ripple current of $i_P + i_S$ is 2.09 A, and its RMS value is 551 mA. Moreover, Figure 28b shows that the stacked buck converter using the low output ripple dead time modulation has a peak-to-peak ripple

current of $i_P + i_S$ of 559 mA and its RMS value is 91 mA. The implementation results show that the use of the low output ripple dead time modulation can significantly reduce the current ripple of $i_P + i_S$.



(**a**) (**b**)

Figure 30. Measured waveforms of the switching node voltage, sum of inductor current ripple and output current using the low output ripple dead time modulation e: (**a**) dead time interval: t_1~t_2; (**b**) dead time interval: t_3~t_{0+T}. [scale v_P (Ch1): 200 V/div; $i_P + i_S$ (*AC*) (Ch2): 5 A/div; v_S (Ch3): 200V/div; i_O (Ch4): 1A/div; time: 80 ns/div].



(**a**) (**b**)

Figure 31. Measured waveforms of the switching node voltage and inductor current: (**a**) conventional dead time; (**b**) low output ripple dead time modulation. (scale v_P (Ch1): 200 V/div; $i_P + i_S(AC)$ (Ch2): 1 A/div; v_S (Ch3): 200V/div; i_O (Ch4): 1A/div; time: 2 µs/div).

8. Conclusions

This study aims to apply low output current ripple, comprehensively discuss existing solutions, and review their advantages and disadvantages. To save the volume of the converter and increase the transient response of the system at medium switching frequencies, a stacked buck converter was eventually selected to meet the requirements of eliminating current ripples under any duty cycle and reducing the inductance of magnetic components. Individual improvements were made to enhance the transient response and current ripple elimination function.

In terms of increasing transient response, this research proposes a boundary limit control method to replace the existing RC delay control method. The proposed method avoids the specific shortcoming that the RC delay control method cannot accelerate transient response after the compensator is saturated. Simultaneously, the small-signal model of the coupled-inductor stacked buck converter is derived. A complete description of the closed-loop compensation design under the boundary limit control method is also provided with the simulation results as support.

In terms of the current ripple elimination function, a low output ripple dead time modulation is proposed to correct the ripple elimination effect that is reduced owing

to the dead time. The theoretical derivation of the dead time modulation method is properly explained in this research. The simulation and actual results show that the low output ripple dead time modulation can significantly improve the output current ripple elimination effect under the conventional dead time modulation method.

Author Contributions: Conceptualization, C.-C.H.; Data curation, C.-C.H., C.-C.L. and C.-Y.N.; Formal analysis, C.-C.H.; Funding acquisition, H.-J.C.; Investigation, C.-C.H.; Methodology, C.-C.H.; Project administration, C.-C.H.; Software, C.-C.L. and C.-Y.N.; Supervision, C.-C.H.; Validation, C.-C.H., C.-C.L. and C.-Y.N.; Visualization, C.-C.H.; Writing—original draft, C.-C.H.; Writing—review & editing, C.-C.H., Y.-C.L. and H.-J.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Informed Consent Statement: Informed consent was obtained from all subjects involved in the study.

Data Availability Statement: Data available in a publicly accessible repository.

Acknowledgments: Thanks to Chroma ATE, Inc. for technical exchange and financial support in the industry-university cooperation case.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Cusenza, M.A.; Bobba, S.; Ardente, F.; Cellura, M.; Di Persio, F.T. Energy and Environmental Assessment of a Traction Lithium-Ion Battery Pack for Plug-in Hybrid Electric Vehicles. *J. Clean. Prod.* **2019**, *215*, 634–649. [CrossRef] [PubMed]
2. Zeng, X.; Li, M.; Abd El-Hady, D.; Alshitari, W.; Al-Bogami, A.S.; Lu, J.; Amine, K. Commercialization of Lithium Battery Technologies for Electric Vehicles. *Adv. Energy Mater.* **2019**, *9*, 1900161. [CrossRef]
3. Miao, Y.; Hynan, P.; von Jouanne, A.; Yokochi, A. Current Li-Ion Battery Technologies in Electric Vehicles and Opportunities for Advancements. *Energies* **2019**, *12*, 1074. [CrossRef]
4. Dehghani-Sanij, A.R.; Tharumalingam, E.; Dusseault, M.B.; Fraser, R. Study of Energy Storage Systems and Environmental Challenges of Batteries. *Renew. Sustain. Energy Rev.* **2019**, *104*, 192–208. [CrossRef]
5. Mehrjerdi, H.; Hemmati, R. Modeling and Optimal Scheduling of Battery Energy Storage Systems in Electric Power Distribution Networks. *J. Clean. Prod.* **2019**. [CrossRef]
6. Li, X.; Wang, S. A Review on Energy Management, Operation Control and Application Methods for Grid Battery Energy Storage Systems. *CSEE J. Power Energy Syst.* **2019**. [CrossRef]
7. Cheng KW, E.; Divakar, B.P.; Wu, H.; Ding, K.; Ho, H.F. Battery-Management System (BMS) and SOC Development for Electrical Vehicles. *Ieee Trans. Veh. Technol.* **2011**, *60*, 76–88. [CrossRef]
8. Elsayed, A.T.; Lashway, C.R.; Mohammed, O.A. Advanced Battery Management and Diagnostic System for Smart Grid Infrastructure. *IEEE Trans. Smart Grid* **2016**, *7*, 897–905. [CrossRef]
9. Ali, M.U.; Zafar, A.; Nengroo, S.H.; Hussain, S.; Junaid Alvi, M.; Kim, H.-J. Towards a Smarter Battery Management System for Electric Vehicle Applications: A Critical Review of Lithium-Ion Battery State of Charge Estimation. *Energies* **2019**, *12*, 446. [CrossRef]
10. Zhang, S.; Guo, X.; Dou, X.; Zhang, X. A Rapid Online Calculation Method for State of Health of Lithium-Ion Battery based on Coulomb Counting Method and Differential Voltage Analysis. *J. Power Sources* **2020**, *479*, 228740. [CrossRef]
11. Gismero, A.; Schaltz, E.; Stroe, D.I. Recursive State of Charge and State of Health Estimation Method for Lithium-Ion Batteries Based on Coulomb Counting and Open Circuit Voltage. *Energies* **2020**, *13*, 1811. [CrossRef]
12. Mayer, R.; Berrehil El Kattel, M.; Oliveira, S.V.G. Multi-Phase Interleaved Bidirectional DC/DC Converter with Coupled Inductor for Electrified-Vehicle Applications. *IEEE Trans. Power Electron.* **2020**, *36*, 2533–2547. [CrossRef]
13. Wong, P.L.; Xu, P.; Yang, P.; Lee, F.C. Performance Improvements of Interleaving VRMs with Coupling Inductors. *IEEE Trans. Power Electron.* **2001**, *16*, 499–507. [CrossRef]
14. Ting, C.Y.; Ko, C.C.; Lin, J.Y.; Chen, C.C.P. An Inductor Current Balancing Technique for FLDLL Based Four-phase Buck Converter with Transient-modulated Constant On-time Control for Load Transient Response. In Proceedings of the 2019 4th International Conference on Intelligent Green Building and Smart Grid (IGBSG), Yi-chang, China, 6–9 September 2019. [CrossRef]
15. Mahmud, M.H.; Zhao, Y.; Zhang, Y. A Sliding Mode Duty-ratio Control with Current Balancing Algorithm for Interleaved Buck Converters. In Proceedings of the 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 4–8 March 2018. [CrossRef]
16. Schutten, M.J.; Steigerwald, R.L.; Sabate, J.A. Ripple Current Cancellation Circuit. In Proceedings of the Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition, Miami Beach, FL, USA, 9–13 February 2003. [CrossRef]
17. Nag, S.S.; Mishra, S.; Joshi, A. A Passive Filter Building Block for Input or Output Current Ripple Cancellation in a Power Converter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *4*, 564–575. [CrossRef]

18. Huang, C.-C. A Wide-Output-Range Bi-directional DC-DC Converter with High-Bandwidth and Low-Switching-Noise Features. Ph.D. Thesis, Electronic and Computer Engineering. National Taiwan University of Science and Technology, Taipei, Taiwan, 2019.
19. Wibben, J.; Harjani, R. A High-Efficiency DC–DC Converter Using 2 nH Integrated Inductors. *IEEE J. Solid-State Circuits* **2008**, *43*, 844–854. [CrossRef]
20. Guilbert, D.; Sorbera, D.; Vitale, G. A Stacked Interleaved DC-DC Buck Converter for Proton Exchange Membrane Electrolyzer Applications: Design and Experimental Validation. *Int. J. Hydrogen Energy* **2019**, *45*, 64–79. [CrossRef]
21. Carsten, B.W. Computer Products Inc. Ripple Cancellation Circuit with Fast Load Response for Switch Mode Voltage Regulators with Synchronous Rectification. US Patent 5,929,692, 27 July 1999.
22. Liu, P.; Liao, C.; Kuo, M. A Spur-Reduction DC–DC Converter With Active Ripple Cancelation Technique. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *6*, 2206–2214. [CrossRef]